

The Itsy Pocket Computer Version 1.5 Hardware Description

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Abstract

The *Itsy pocket computer* is a flexible research platform developed at Compaq Computer Corporation's *Western Research Laboratory (WRL)*. Its aim is to enable hardware and software research in pocket computing, including low-power hardware, power management, operating systems, wireless networking, user interfaces, and applications. This document describes the architecture, the hardware, and the low-level programming model of the Itsy computer.

Revision 1.0

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1 Introduction

This document is an extended version of *The Itsy Pocket Computer Version 1.5: User's Manual* [Vir98]. Besides describing the architecture and the programmer's model of the *itsy pocket computer*, it also provides information on the hardware design. It is aimed at low-level software developers and daughter-card designers, as well as experimenters who need to analyze, customize, or modify the Itsy hardware.

1.1 History

The first *printed-circuit board (PCB)*, referred to as *itsy mother-board version 1.0*, was completed in November 1997. This first prototype had several flaws, all of which could, fortunately, be corrected. The logic design corresponding to a modified (i.e., patched) version 1.0 board is known

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as *Itsy mother-board version 1.1*. This design corresponds only to a set of schematics, no physical PCB having been manufactured. A total of six version 1.0/1.1 systems were built.

A second prototype, named *Itsy mother-board version 1.5* was first built in March 1998. It corresponds to a version 1.1 system with a few additional features. From the programmer's point-of-view, there are almost no differences between the versions 1.1 and 1.5.

This document describes the Itsy mother-board version 1.5. All relevant differences between the versions 1.1 and 1.5 are outlined in foot-notes.

1.2 Notations

In this report, electrical signals are represented as upper-case names in a sans-serif font (e.g., PWR_EN). Active-low signals are denoted by over-lines (e.g., $\overline{\text{RESET}}$), while buses and element of buses are specified by subscripts (e.g., $D_{31..0}$, A_0). In the schematics and PLD listing, the same signals are represented using the syntax and conventions of the corresponding CAD tools. For example, the signal $\overline{\text{CS}}_0$ appears as `~cs[0]` in the schematics, according to the WindowSIL [Tha97] conventions, and is represented as `!CS0` in the PLD listing, following the ABEL syntax of Synario [Syn96].

On the schematics, each component is uniquely identified by a short reference (2–4 letters). In this document, these component references are represented in a fixed-size font (e.g., `s01`).

2 Architecture

Figure 1 presents the architecture of the Itsy computer. The left part of the figure shows the implementation of the Itsy mother-board. The right part of the figure represents all the resources available through the daughter-card interface (see Section 2.7). Figure 2 shows the front panel of the Itsy computer and the placement of input/output units. The remainder of this section describes each individual unit.

2.1 Processor

The *central processing unit (CPU)* of the Itsy computer is the StrongARM SA-1100 processor (`u06`), developed by Digital Equipment Corporation's Digital Semiconductor division, which became part of Intel in May 1998. A good knowledge of the manufacturer's documentation [DEC98a, DEC98b] is assumed throughout this report.

The main crystal (`x1`) frequency is 3.6864 MHz. Using the processor's *phase-locked loop (PLL)*, this makes it possible to vary the CPU core frequency from 59.0 MHz to 206.4 MHz. The real-time crystal (`x2`) frequency is 32.768 kHz. On the Itsy mother-board version 1.5, it is possible to use an external source for either clock by removing the crystal `x1` or `x2` and connecting a signal of appropriate frequency and amplitude to the test point `t13` or `t15`, respectively. The test points `t12` and `t14` provide nearby connections to ground (GND).¹

¹On the Itsy mother-board version 1.1, the test points `t08` (main clock) and `t10` (real-time clock) should be used instead, while the test points `t07` and `t09` provide nearby connections to ground (GND).

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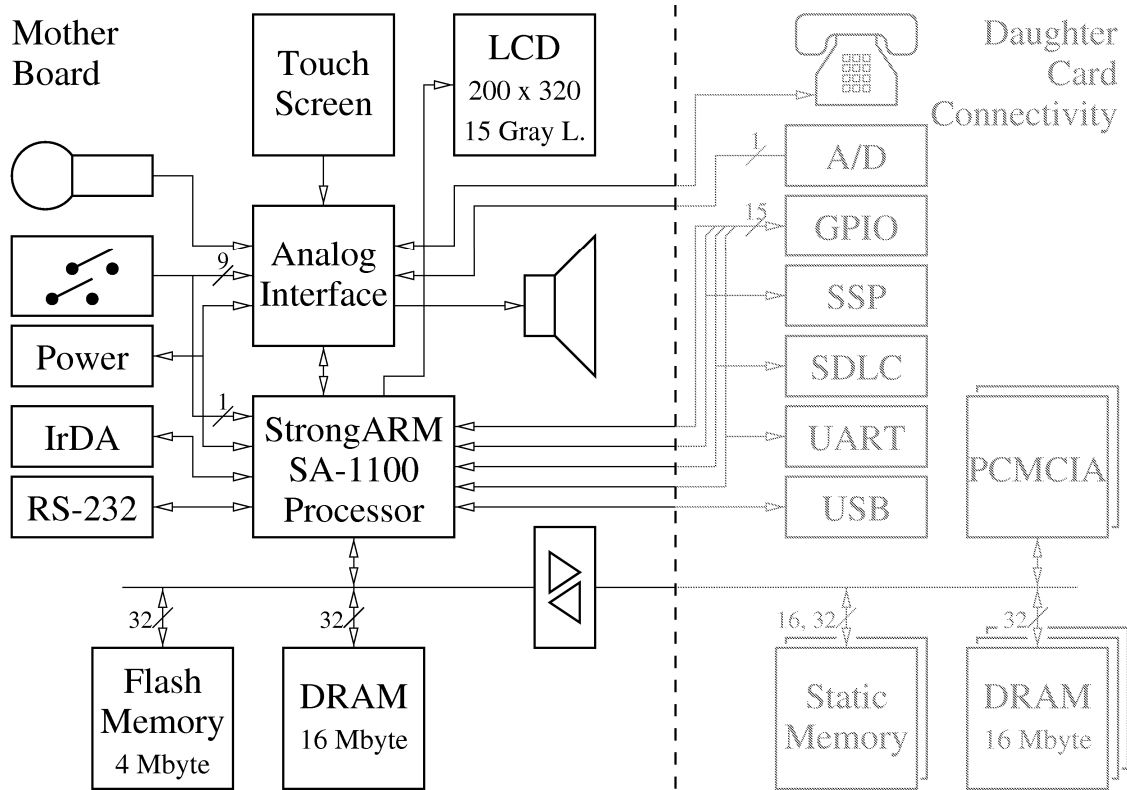


Figure 1: Architecture of the Itsy pocket computer.

2.2 Power supply

The Itsy computer is powered by a pair of standard AAA alkaline batteries, supplying a voltage V_{batt} . A measurement device enables external monitoring of the power consumption (see below). The voltage after this device is referred to as V_{pwrin} . For most practical purposes, these two voltage can be considered equal (i.e., $V_{\text{batt}} \approx V_{\text{pwrin}}$). With new batteries, the maximum battery voltage is $V_{\text{batt}} \approx 3.2 \text{ V}$. On the Itsy mother-board version 1.5, an external power supply (i.e., $2.0 \text{ V} < V_{\text{batt}} \leq 3.3 \text{ V}$) can be connected using the serial-interface connector (j5) (see Section 2.6.3).² Since, there is no mechanism to automatically disconnect the batteries when an external power supply is used, the batteries must be removed before connecting the external power supply. Failure to do this carries a risk of leakage and possibly fire.

Two voltages are regulated from the batteries or external power supply: the main power-supply voltage V_{dd} (3.3 V nominal) and the CPU core power-supply voltage V_{cc} (1.5 V nominal). These voltages can be adjusted using two trim potentiometers (p1 and p2, respectively). The system is designed such that, accounting for the component tolerances, the voltage range for V_{dd} is at least $[3.08 \text{ V} .. 3.36 \text{ V}]$ and at most $[2.73 \text{ V} .. 3.60 \text{ V}]$. Similarly, the voltage range for V_{cc} is at least

²This feature is not available on the Itsy mother-board version 1.1.

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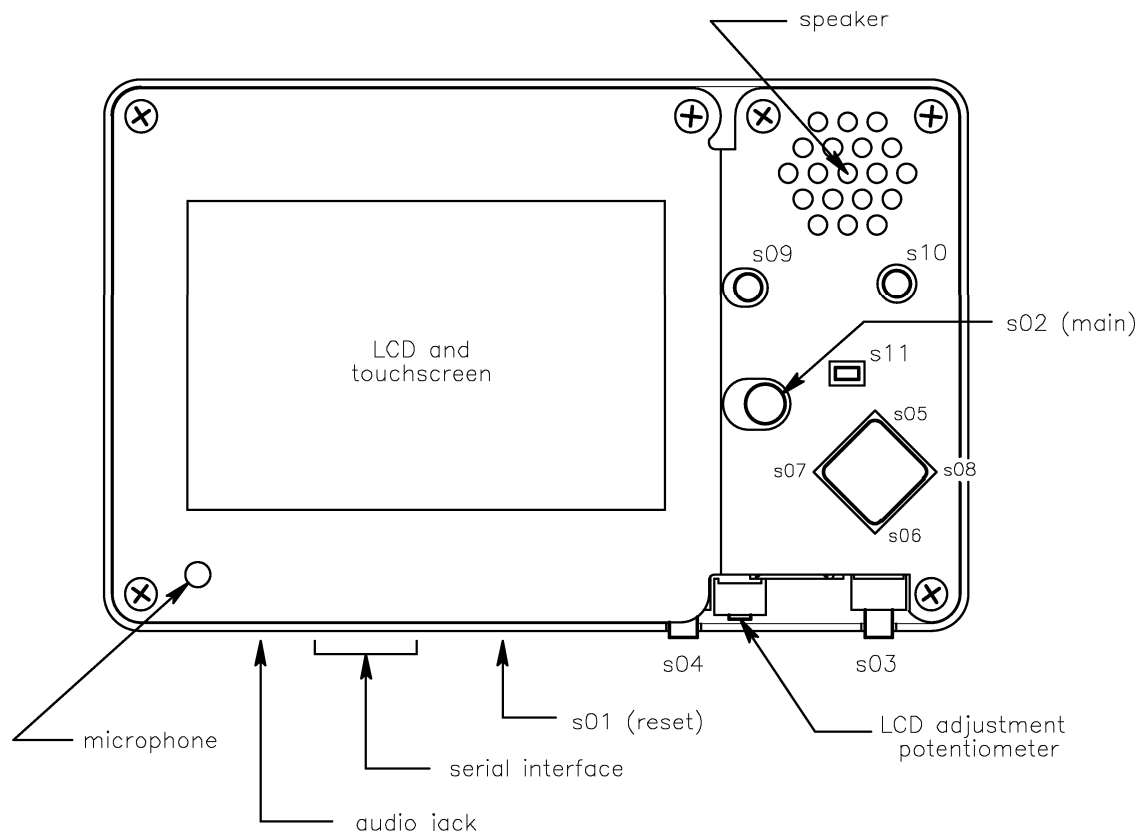


Figure 2: Front panel of the Itsy computer.

[1.50 V .. 2.02 V] and at most [1.37 V .. 2.15 V].

On the Itsy mother-board version 1.5, three precision 20 mΩ resistors, shown in Figure 3, are provided to enable experimenters to measure the current drawn at the voltages V_{batt} (or V_{pwrin}), V_{dd} , and V_{cc} . The batteries or the external power supply are connected to the signal BATT (i.e., V_{batt}), which is in turn connected to the signal PWRIN (i.e., V_{pwrin}) by the 20 mΩ resistor r03. Since, all other units are connected to the signal PWRIN, the total current flows through the resistor r03. The test points t02 and t03 are connected to the signals BATT and PWRIN, respectively. The test point t01 provides a nearby connection to ground (GND). Similarly, the 3.3 V and 1.5 V nominal power supply are generated on the signals PWR33 and PWR15, which are connected to the signals P3300 (i.e., V_{dd}) and P1500 (i.e., V_{cc}) by the 20 mΩ resistors r49 and r50, respectively. The test points t05, t06, t08, and t09 are connected to the signals PWR33, P3300, PWR15, and P1500, respectively, while the test points t04 and t07 provide nearby connections to ground (GND).³

³On the Itsy mother-board version 1.1, only the 20 mΩ resistor r03 is available to measure the current drawn at the voltage V_{batt} (or V_{pwrin}). The test points t01 and t02 are connected to the signals BATT and PWRIN, respectively. There is no support to measure the current drawn at the voltages V_{dd} and V_{cc} . The test points t03 and t05 are connected to the signals P3300 and P1500, respectively, while the test points t04 and t06 provide nearby connections to ground (GND).

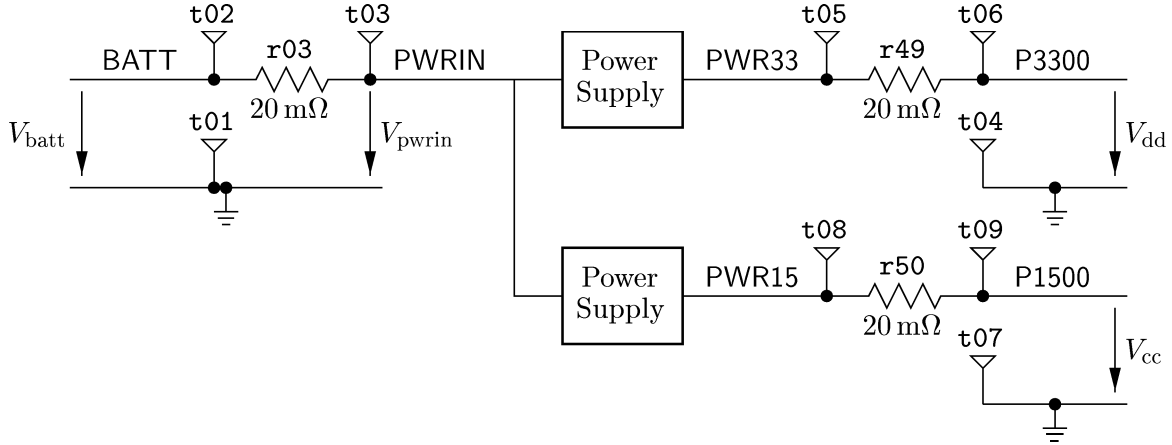


Figure 3: Precision resistors for current measurement (Itsy mother-board version 1.5).

During sleep mode, the V_{dd} power supply is switched to a more efficient low-current mode, while the V_{cc} power supply is disabled. This behavior is achieved by connecting the respective control signals PWRSEL and PWREN to the signal PWR_EN of the StrongARM SA-1100 processor (u06) [DEC98b] through the 0Ω resistors r11 and r15, respectively. For certain applications, it may be necessary to keep the V_{dd} power supply in high-current mode and/or to keep the V_{cc} power supply enabled during sleep mode. This can respectively be achieved by removing the 0Ω resistor r11 or r15 and replacing the $\infty\Omega$ resistor r10 or r14 with a 0Ω resistor.

2.2.1 Power monitoring

The Itsy computer features several mechanisms to monitor the power-supply voltages. At the hardware level, the signals BATT_FAULT and VDD_FAULT of the StrongARM SA-1100 processor (u06) [DEC98b] force a transition to sleep mode if the voltage V_{pwrin} falls below the threshold $V_{pwrin, fault}$ (i.e., $V_{pwrin} \leq V_{pwrin, fault} \approx 2.0\text{ V}$) or if the voltage V_{dd} falls below the threshold $V_{dd, fault}$ (i.e., $V_{dd} \leq V_{dd, fault} \approx 2.7\text{ V}$), respectively. Table 1 gives the voltage tolerances for the thresholds $V_{pwrin, fault}$ and $V_{dd, fault}$. Although there is no mechanism to monitor the voltage V_{cc} , the corresponding power supply has been designed such that this voltage should always remain stable as long as the battery voltage V_{pwrin} is above the threshold $V_{pwrin, fault}$.

Voltage threshold	Min.	Typ.	Max.
$V_{pwrin, fault}$	1.88 V	1.93 V	1.98 V
$V_{dd, fault}$	2.58 V	2.67 V	2.76 V
$V_{dd, low}$	2.82 V	2.91 V	3.01 V

Table 1: Voltage thresholds for power monitoring.

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The input signal GPIO₂ (PWROK) is set to 1 during normal operation and toggles to 0 if the main power-supply voltage V_{dd} drops below the threshold $V_{dd,low}$ (i.e., $V_{dd} \leq V_{dd,low} \approx 3.0\text{ V}$), given in Table 1 (see Section 3.2). This signal can be polled by software or used to generate an interrupt. A software transition to sleep mode can then be forced, after the current state has been saved as appropriate. As shown in Table 1, the signal GPIO₂ (PWROK) will always toggle to 0 before the signal VDD_FAULT is asserted. Since most components (including the processor) are not specified to operate correctly at a voltage V_{dd} lower than 3.0 V, the signal GPIO₂ (PWROK) must be monitored. The signal VDD_FAULT should only be considered as a “safety” mechanism.

Finally, the three voltages V_{pwrin} , V_{dd} , and V_{cc} are connected to the general-purpose analog input pins AD₀, AD₁, and AD₂ of the UCB1200 analog interface (u18) [Phi97b] and can be measured using the corresponding analog-to-digital converters. Since there is no early warning that the battery voltage V_{pwrin} is about to reach the threshold $V_{pwrin,fault}$, the software must use this interface to infer the state of the batteries.

2.3 Reset scheme

A reset pulse is applied to the signal $\overline{\text{RESET}}$ upon power-up or when the reset push-button (s01) is pressed (see Figure 2). This signal is also asserted when the power-supply voltage V_{dd} falls below a level that is at least 30 mV lower than the threshold $V_{dd,fault}$. This should only happen at the very end of the batteries’ life, when the voltage V_{batt} (or V_{pwrin}) is so low that the power supply is unable to keep the voltage V_{dd} regulated even at low sleep-mode current.

On the Itsy mother-board version 1.5, it is possible to install a second reset push-button (s12) for experimenters who need a convenient way to reset the Itsy computer. It is also possible to generate a reset by setting the test point t11 to 0. The test point t10 provide a nearby connection to ground (GND).⁴

2.4 Control logic

An external controller, implemented using a Philips PZ3032-8BC *programmable logic device (PLD)* (u08a) [Phi97a] is used to select the boot memory and to implement the *auxiliary LCD controller*. Since the PZ3032-8BC PLD (u08a) is housed in a *thin quad flat package (TQFP)* and is directly soldered on the PCB, it is awkward to re-program this device. Experimenters, who need the flexibility of re-programming this controller, can replace this device with a socket and the PZ3032-8A44 PLD (u08b), which is housed in a *plastic leaded chip carrier (PLCC) package*.

Static-memory bank 0 mirrors either bank 1 or bank 2, depending whether the StrongARM SA-1100 processor (u06) [DEC98b] should boot⁵ from the mother-board or from the daughter-card (see Sections 2.7 and 3.2). After a hardware reset (i.e., power-up or push-button reset) or while exiting sleep mode, the daughter-card signal $\overline{\text{DCBOOT}}$ and the processor signal GPIO₁₉ (DCEN)

⁴Neither the second reset push-button (s12) nor the test points t10 and t11 are available on the Itsy mother-board version 1.1.

⁵The initialization sequence that follows a reset (i.e., hardware, software, or watch-dog reset) is very similar to the sequence that is executed while exiting sleep mode. Thus, for the sake of simplicity, the verb “boot” is used in this document as a generic term to refer to any of these actions.

are sampled.⁶ If the former signal is asserted (0) and the latter signal is set to 1, static-memory bank 0 mirrors bank 2 and the processor boots from the daughter-card. Otherwise, bank 0 mirrors bank 1 and the processor boots from the mother-board. After a hardware reset, the boot memory is solely selected by the signal $\overline{\text{DCB}\overline{\text{OOT}}}$, since the value of the signal GPIO₁₉ (DCEN) is always 1 (see Section 3.2).

The auxiliary LCD controller makes it possible to capture a black-and-white image (no grey levels) on the LCD and to maintain it even when the processor is in sleep mode (see Section 2.6.1). With the signal GPIO₂₀ (LCDEN) set to 1 and the signal GPIO₂₁ (AUXLCDEN) set to 0 (see Section 3.2), the software should display a black-and-white image on the LCD using the processor's LCD controller. The signal GPIO₂₁ (AUXLCDEN) should then be toggled to 1. After the complete image has been transmitted, it is captured and remains displayed as long as the signals GPIO₂₀ (LCDEN) and GPIO₂₁ (AUXLCDEN) both stay at 1. The exact capture time occurs at the first end-of-frame that the value of the signal GPIO₂₁ (AUXLCDEN) is 1.

2.5 Memory system

On the mother-board, the memory system consists of a *flash memory* decoded as static-memory bank 1 and of *dynamic random-access memory (DRAM)* bank 0. Static-memory banks 2 and 3 as well as DRAM banks 1, 2, and 3 are available to the daughter-card interface (see Section 2.7). Static-memory bank 0—from which the StrongARM SA-1100 processor (u06) [DEC98b] boots—mirrors either bank 1 or bank 2 (see Sections 2.4, 2.7, and 3.2).

2.5.1 Flash memory

A pair of 16-bit flash-memory circuits (u09 and u10) implement the 32-bit mother-board flash memory. Many different devices can be accommodated:

AMD Am29LV160B *OssPT* [AMD97e]
 AMD Am29LV800 *O-ssPT*/Am29LV800B *OssPT* [AMD97c, AMD97d]
 AMD Am29LV400 *O-ssPT* [AMD97a]
 AMD Am29LV200 *O-ssPT* [AMD97b]
 Hitachi HN29V *O800P-ss*/HN29W *O800P-ss* [Hit97c, Hit97d]
 Motorola M29F800A2 *OPss*/M29F800A3 *OPss* [Mot97]
 Sharp LH28F800SGP-*Lss* [Sha97]

where “*O*” specifies the internal sector organization, “*ss*” specifies the speed, “*P*” specifies the package, and “*T*” specifies the temperature range. Any other compatible parts can also be used.

Following the convention described in Sections 2.7.1 and 3.3, a non-volatile memory identification structure describes the characteristics of the specific parts used on a given system and hence allows the software to configure the memory interface correctly.

The *reset/power-down pin* of the flash-memory circuits (u09 and u10) is asserted (0) during a reset (i.e., hardware, software, or watch-dog reset) and during sleep mode. When the flash memory does not need to be accessed, this signal can also be asserted (0) by setting the signal GPIO₃

⁶On the Itsy mother-board version 1.1, these signals are also sampled after a software or watch-dog reset.

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($\overline{\text{FLFOFF}}$) to 0 (see Section 3.2). When the Itsy computer must boot from the mother-board, this signal should never be set to 0 during sleep mode, since the processor would be unable to read the boot memory upon wake up. This can easily be achieved by setting bit 3 of the *power manager GPIO sleep state register* PGSR of the StrongARM SA-1100 processor (u06) [DEC98b] to 1.

The *ready/not-busy pins* of the flash-memory circuits (u09 and u10) can be monitored using the signals GPIO₄ (FL0RY/BY), for the least significant 16 data bits D_{15..0}, and GPIO₅ (FL1RY/BY), for the most significant 16 data bits D_{31..16} (see Section 3.2).

The hardware write-protection mechanism, featured by some of the supported parts, is never used, and the corresponding pin is always de-asserted (1).

2.5.2 Dynamic RAM

A pair of 64 Mbit (i.e., 2^{12} rows \times 2^{10} columns \times 16 bits) self-refresh DRAM circuits (u11 and u12) implement the 32-bit mother-board DRAM. Many different *fast-page mode* or *enhanced data out* (EDO) devices can be accommodated:

Hitachi HM5165160ALTT-ss [Hit97a]

Hitachi HM5165165ALTT-ss [Hit97b]

Samsung KM416V4100AS-Lss/KM416V4100BS-Lss [Sam97a, Sam98a]

Samsung KM416V4104AS-Lss/KM416V4104BS-Lss [Sam97b, Sam98b]

Toshiba TC5165165AFTS-ss [Tos96]

where “ss” specifies the speed. Any other compatible parts can also be used.

Since—unlike with the flash memory—the software can not recognize which are the specific parts used on a given system, all Itsy computers version 1.5 have been assembled using the fastest available parts, that is, 50 ns EDO DRAM circuits (KM416V4104AS-L5, KM416V4104BS-L5, or TC5165165AFTS-50).

The choice of the mother-board DRAM affects which types of DRAM can be used on a daughter-card. Since all banks must have the same number of rows, only parts with 2^{12} rows can be considered. Moreover, since all banks must be accessed at the speed of the slowest one, it is best to use the same type of circuits everywhere.

2.6 Input/output devices

This section describes the different input/output units of the Itsy mother-board. All analog devices are handled by the Philips UCB1200 analog interface (u18) [Phi97b]. This circuit is connected to StrongARM SA-1100 processor (u06) [DEC98b] using the *Multi-media Communications Port* (MCP) engine of serial port 4.

2.6.1 Display and touch-screen

The display of the Itsy computer is an Epson TCM-A0822-*xx* *liquid crystal display (LCD)* [Eps97], where “*xx*” specifies the revision. It features 200 lines of 320 pixels each. The interface is 8 bits wide. The LCD controller of the StrongARM SA-1100 processor (u06) [DEC98b] is used as the main controller. It can display 15 levels of grey. A trim potentiometer (p3) is used to control the brightness of the LCD (see Figure 2).

The signal GPIO₂₀ (LCDEN) is connected to the enable pins $\overline{\text{DOFF1}}$ and $\overline{\text{DOFF2}}$ of the LCD (see Section 3.2). The LCD is enabled when this signal is set to 1 and disabled when it is set to 0. Similarly, the signal GPIO₂₁ (AUXLCDEN) is used to control an auxiliary LCD controller, which makes it possible to maintain a black-and-white image (no grey levels) on the LCD, even when the processor is in sleep mode (see Sections 2.4 and 3.2). The auxiliary LCD controller is enabled when this signal is set to 1 and disabled when it is set to 0. To capture a black-and-white image, the image should be displayed using the processor’s LCD controller with the auxiliary LCD controller disabled. The signal GPIO₂₁ (AUXLCDEN) should then be toggled to 1. After the complete image has been transmitted, it is captured and remains displayed as long as the signals GPIO₂₀ (LCDEN) and GPIO₂₁ (AUXLCDEN) both stay at 1.

In order to allow experiments with different types of LCDs, the unused processor signal L_BIAS can be connected to pin 6 of the LCD connector (j3), by replacing the $\infty \Omega$ resistor r47 with a 0Ω resistor.

On the Itsy mother-board version 1.5, the four signals TSXP, TSXN, TSYP, and TSYN of the resistive touch-screen are directly connected to the TSPX, TSMX, TSPY, and TSMY pins of the UCB1200 analog interface (u18) [Phi97b], respectively.⁷

In order to minimize the noise generated by the LCD, it is possible to synchronize the sampling of the touch-screen voltages with the LCD line pulse. The synchronization signal TSCRS MPL — connected to the ADCSYNC pin of the UCB1200 analog interface (u18) — is identical to the LCD line clock LCDLCLK. On the Itsy mother-board version v 1.5, the signals LCDLCLK and TSCRS MPL are connected by the 0Ω resistor r51.⁸

2.6.2 Audio interface

The audio interface consists of a microphone (j7), a speaker (j8), and a 3-contact 2.5 mm jack connector (j6) (see Figure 2). The mother-board microphone (j7) and speaker (j8) are disconnected when the jack connector (j6) is used. Table 2 provides the pin-out of this connector.

The audio input is connected to the MICP pin of the UCB1200 analog interface (u18) [Phi97b], through a $1 \mu\text{F}$ decoupling capacitor (c74). The negative terminal of the mother-board microphone (j7) is connected to the MICGND pin (shown as MICN on the schematics) of the UCB1200 analog interface (u18). When an external microphone is used, its negative terminal is connected to the system ground (GND).

⁷On the Itsy mother-board version 1.1, the signals TSXP, TSXN, TSYP, and TSYN of the touch-screen are connected to the TSMX, TSPX, TSPY, and TSMY pins of the UCB1200 analog interface (u18), respectively (i.e., the polarity of the X-axis is inverted).

⁸On the Itsy mother-board version v 1.1, the signal TSCRS MPL is directly generated by the PZ3032-8BC PLD (u08a).

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Pin	Signal	Function	Dir.
1	GND	Ground (common terminal)	
2	MIC	Microphone (audio input)	I
3	SPKR	Speaker (audio output)	O

Table 2: Audio jack connector (j8) pin-out. Pin 1 is the sleeve, pin 2 is the tip, and pin 3 is the ring (i.e., middle contact).

Similarly, the audio output is connected to the SPKRP pin of the UCB1200 analog interface (u18), through a $47\mu\text{F}$ decoupling capacitor (c75). The negative terminal of the mother-board speaker (j8) is connected to the SPKRN pin of the UCB1200 analog interface (u18), allowing differential drive of the speaker. When an external speaker is used, its negative terminal is connected to the system ground (GND). In this case, the speaker is no longer differentially driven. It is possible to connect the ground of the mother-board speaker (j8) to the system ground (GND), by removing the 0Ω resistor r45 and by replacing the $\infty\Omega$ resistor r46 with a 0Ω resistor.

2.6.3 Serial interface

Serial port 3 of the StrongARM SA-1100 processor (u06) [DEC98b] provides the *universal asynchronous receiver/transmitter (UART)* engine that is used as the RS-232 interface of the Itsy mother-board (see Figure 2). It is connected to a Hirose 3260-8S1 connector (j5) through a Maxim MAX3223CAP RS-232 driver (u20) [Max96].

The choice of a non-standard serial-interface connector (j5) for the serial interface has been made in order to decrease the size of the Itsy computer. Table 3 provides the pin-out of this connector. On the Itsy mother-board version 1.5, it can also be used to connect to an external power supply (see Section 2.2).⁹

A consequence of having a non-standard connector is that special cables must be used. Figure 4 shows the connection from the serial-interface connector (j5) to a 6-pin male MMJ connector. The same cable can be used to connect the Itsy computer either to a *data communication equipment (DCE)*, i.e., a modem, or to a *data terminal equipment (DTE)*, i.e., a computer or a terminal. Figure 5 presents two examples of connection to 9-pin DIN connectors. The cable represented by Figure 5(a) is used to connect the Itsy computer to a DCE, while the cable represented by Figure 5(b) is used to connect the Itsy computer to a DTE. It can be noted that an MMJ cable (see Figure 4) used in conjunction with the DEC H8571-J MMJ-to-DIN adapter corresponds to the connection described by Figure 5(b). Some applications might require different connections and, hence, use different cables.

The signals GPIO_{23} (UARTFOFF) and GPIO_{24} (UARTFON) control the MAX3223CAP RS-232 driver (u20) (see Section 3.2). When the former signal is set to 0, the driver is disabled. When it is set to 1, the driver is either enabled or in *AutoShutdown mode*, depending whether the signal GPIO_{24} (UARTFON) is set to 1 or to 0, respectively. In AutoShutdown mode, the driver enables and disables itself depending whether a valid RS-232 input signal is detected (i.e., the serial interface

⁹This feature is not available on the Itsy mother-board version 1.1.

The Itsy Pocket Computer Version 1.5: Hardware Description

Pin	Signal	Function	Dir.
1	RSDTR	RS -232 interface d ata t erminal r eady (DTR)	O
2	BATT *	B attery voltage V_{batt}	
3	RSTXD	RS -232 interface t ransmit d ata (TxD)	O
4	GND	G round	
5	GND	G round	
6	RSRXD	RS -232 interface r ecieve d ata (RxD)	I
7	BATT *	B attery voltage V_{batt}	
8	RSDSR	RS -232 interface d ata s et r eady (DSR)	I

* On the Itsy mother-board version 1.1, pins 2 and 7 are connected to ground (GND).

Table 3: Serial-interface connector (j5) pin-out.

is connected to a powered system) or not (i.e., the serial interface is unconnected or is connected to a unpowered system). When the driver is disabled in AutoShutdown mode, transmitting data will not enable it. As a consequence, a potential dead-lock might happen when the serial interface is connected to another similar interface (e.g., when two Itsy computers are connected together), since both drivers might remain disabled. To avoid this, the software should briefly set the signal GPIO₂₄ (UARTFON) to 1 when establishing a connection. The driver can then be switched to AutoShutdown mode by toggling this signal to 0.

The signal GPIO₇ (UARTVALID) is set to 1 when a valid RS-232 input signal is detected and to 0 when no valid signals are detected (see Section 3.2).

The signals GPIO₈ (UARTDSR) and GPIO₉ (UARTDTR) are connected to the second receive and transmit buffers of the MAX3223CAP RS-232 driver (u20) (see Section 3.2). Used in conjunction with an appropriate special cable, they can emulate one additional input signal and one additional output signal of the RS-232 standard. In the examples presented in Figures 4 and 5, they are shown to emulate the *data set ready* signal DSR and the *data terminal ready* signal DTR, respec-

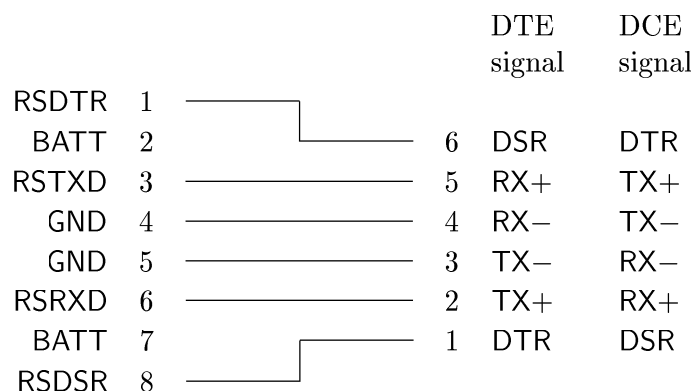


Figure 4: Serial-interface cable to 6-pin male MMJ connector.

The Itsy Pocket Computer Version 1.5: Hardware Description

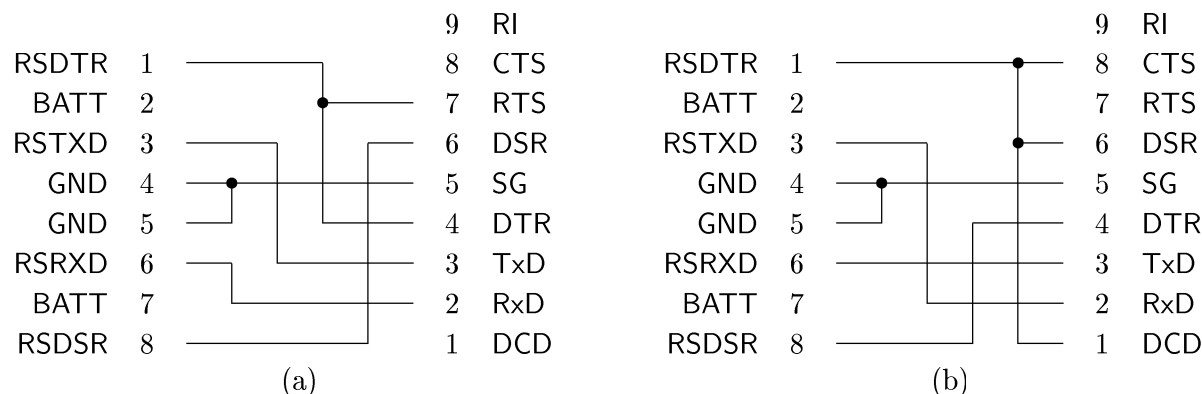


Figure 5: Serial-interface cables to 9-pin male and female DIN connectors. (a) Connection from the Itsy computer to a DCE (9-pin male DIN connector). (b) Connection from the Itsy computer to a DTE (9-pin female DIN connector, null-modem cable).

tively. However, since they are general-purpose input/output signals and since the serial-interface connector (j5) is non-standard, there are no restrictions on which signals they can emulate. For example, some applications might use these signals to emulate the *clear to send* signal CTS and the *request to send* signal RTS.

2.6.4 Infrared interface

The infrared interface of the Itsy computer is implemented by a Novalog MiniSIR2 IrDA transceiver (u19) [Nov98], used in conjunction with the UART engine of serial port 2 of the StrongARM SA-1100 processor (u06) [DEC98b]. This interface is compliant with the *Infrared Data Association (IrDA)* standard version 1.0. Only the UART engine of serial port 2 should be used, the *high-speed serial to parallel (HSSP)* engine should never be used. Moreover, the bit rate should be limited to the range: [2.4kbit/s..115.2kbit/s]. Since the receive and transmit pins of the MiniSIR2 IrDA transceiver (u19) are both active high, the *HSSP control register 2* HSCR2 of the StrongARM SA-1100 processor (u06) should be initialized to 000C0000₁₆.

The signal GPIO₂₂ ($\overline{\text{IRDAEN}}$) is used to control the MiniSIR2 IrDA transceiver (u19) (see Section 3.2). The transceiver is enabled when this signal is set to 0 and disabled when it is set to 1.

2.6.5 Push-buttons

The Itsy computer features 10 general-purpose push-buttons (see Figure 2). The *main push-button* (s02) is connected to the signal GPIO₀ ($\overline{\text{MAINPB}}$) of the StrongARM SA-1100 processor (u06) [DEC98b] (see Section 3.2). This signal is set to 0 when the push-button is pressed and to 1 when the push-button is released. This push-button is always enabled. It should be debounced by software. Although this is, otherwise, a general-purpose push-button, it can be used to wake up the processor after a hardware transition to sleep mode due to the assertion of the signal BATT_FAULT or the signal VDD_FAULT (see Section 2.2.1).

The 9 remaining push-buttons (**s03** to **s11**) are connected to the $\text{IO}_{0..8}$ pins of the UCB1200 analog interface (**u18**) [Phi97b]. They are enabled by setting the IO_9 pin to 0 and are disabled when this pin is configured as input or set to 1. The $\text{IO}_{0..8}$ pins are set to 0 when the corresponding push-buttons are pressed and to 1 when they are released. These push-buttons should be debounced by software.

2.7 Daughter-card interface

The aim of the daughter-card interface is to provide hardware designers with all the unused resources of the StrongARM SA-1100 processor (**u06**) [DEC98b] and UCB1200 analog interface (**u18**) [Phi97b]. Daughter-cards are connected to the Itsy mother-board through a 160-pin connector (**j2**). The functionality available through the daughter-card interface includes:

- 2 static-memory banks (banks 2 and 3). It is possible to boot from the daughter-card. In this case, bank 0 mirrors bank 2.
- 3 DRAM banks (banks 1, 2 and 3).
- 2-socket *Personal Computer Memory Card International Association (PCMCIA)* interface.
- 4 serial interfaces: *universal serial bus (USB)*, *universal asynchronous receiver/transmitter (UART)*, *synchronous data link controller (SDLC)*, and *synchronous serial port (SSP)*.
- 15 general-purpose input/output signals, 13 of which can be used for interrupts.
- 1 telecommunication codec (e.g., for software modem).
- 1 general-purpose analog input (10-bit analog-to-digital converter, nominal voltage range: [0 V .. 7.5 V]).

Not all these features are available simultaneously, since three of the serial interfaces (i.e., UART, SDLC, SSP) are allocated by reconfiguring some of the general-purpose input/output pins.

Table 4 shows the pin-out of the daughter-card connector (**j2**). Some signals (mostly the memory bus) are buffered by SN74LVCH16244ADGG drivers (**u13**, **u14**, and **u15**) [TI97a] or SN74LVCH16245ADGG transceivers (**u16** and **u17**) [TI97b]. Buffered signals are explicitly specified as such in the description below. All other signals are unbuffered. All buffers are enabled when the signal GPIO_{19} (DCEN) is set to 1 and disabled when it is set to 0 (see Section 3.2). The following signals are available:

GND: ground

27 pins are used to carry the system's ground.

P3300: power 3.300 V

24 pins are used to carry the 3.3 V-nominal power-supply voltage V_{dd} (see Section 2.2). The amount of current available to daughter-cards varies depending on the processing state of the Itsy computer (i.e., CPU core frequency, enabled/disabled state of all units, etc.). Daughter-cards that do not draw more than 80 mA while the StrongARM SA-1100 processor (**u06**) [DEC98b] is in sleep mode, and do not draw more than 200 mA while the processor is in idle or run modes, can be accommodated in almost any processing states. A further power

The Itsy Pocket Computer Version 1.5: Hardware Description

Pin	Signal	Dir.	Pin	Signal	Dir.	Pin	Signal	Dir.	Pin	Signal	Dir.
1	DCA ₀	O	41	$\overline{\text{DCPWAIT}}$	I	81	P3300		121	GND	
2	DCA ₁	O	42	$\overline{\text{DCIOIS16}}$	I	82	GND		122	DCD ₁₄	I/O
3	P3300		43	GND		83	TINN	I	123	DCD ₆	I/O
4	DCA ₂	O	44	$\overline{\text{DCPREG}}$	O	84	TINP	I	124	DCD ₂₉	I/O
5	DCA ₃	O	45	DCPSKTSEL	O	85	GND		125	DCD ₂₁	I/O
6	GND		46	P3300		86	GND		126	GND	
7	DCA ₄	O	47	GPIO ₁	I/O	87	UDCN	I/O	127	DCD ₁₃	I/O
8	DCA ₅	O	48	$\overline{\text{DCCS}}_2$	O	88	UDCP	I/O	128	DCD ₅	I/O
9	DCA ₆	O	49	P3300		89	GND		129	P3300	
10	DCA ₇	O	50	$\overline{\text{DCPIOW}}$	O	90	RXD ₁	I/O	130	DCD ₂₈	I/O
11	GND		51	$\overline{\text{DCPIOR}}$	O	91	PWRIN		131	DCD ₂₀	I/O
12	DCA ₈	O	52	GND		92	TXD ₁	I/O	132	GND	
13	DCA ₉	O	53	$\overline{\text{DCPWE}}$	O	93	PWRIN		133	DCD ₁₂	I/O
14	P3300		54	$\overline{\text{DCPOE}}$	O	94	P3300		134	DCD ₄	I/O
15	DCA ₁₀	O	55	P3300		95	GPIO ₂₇	I/O	135	P3300	
16	DCA ₁₁	O	56	$\overline{\text{DCPCE}}_2$	O	96	GPIO ₂₆	I/O	136	DCROMSEL	I
17	GND		57	$\overline{\text{DCPCE}}_1$	O	97	P3300		137	$\overline{\text{DCBOOT}}$	I
18	DCA ₁₂	O	58	GND		98	GPIO ₂₅	I/O	138	P3300	
19	DCA ₁₃	O	59	$\overline{\text{DCWE}}$	O	99	GPIO ₁₈	I/O	139	DCD ₂₇	I/O
20	P3300		60	$\overline{\text{DCOE}}$	O	100	P3300		140	DCD ₁₉	I/O
21	$\overline{\text{RESET_OUT}}$	O	61	$\overline{\text{DCCAS}}_3$	O	101	GPIO ₁₇	I/O	141	GND	
22	PWR_EN	O	62	$\overline{\text{DCCAS}}_2$	O	102	GPIO ₁₆	I/O	142	DCD ₁₁	I/O
23	P3300		63	GND		103	P3300		143	DCD ₃	I/O
24	DCA ₁₄	O	64	$\overline{\text{DCCAS}}_1$	O	104	GPIO ₁₅	I/O	144	P3300	
25	DCA ₁₅	O	65	$\overline{\text{DCCAS}}_0$	O	105	GPIO ₁₄	I/O	145	DCD ₂₆	I/O
26	GND		66	P3300		106	P3300		146	DCD ₁₈	I/O
27	DCA ₁₆	O	67	$\overline{\text{DCRAS}}_3$	O	107	GPIO ₁₃	I/O	147	GND	
28	DCA ₁₇	O	68	$\overline{\text{DCRAS}}_2$	O	108	GPIO ₁₂	I/O	148	DCD ₁₀	I/O
29	P3300		69	GND		109	P3300		149	DCD ₂	I/O
30	DCA ₁₈	O	70	$\overline{\text{DCRAS}}_1$	O	110	GPIO ₁₁	I/O	150	DCD ₂₅	I/O
31	DCA ₁₉	O	71	$\overline{\text{DCCS}}_3$	O	111	GPIO ₁₀	I/O	151	DCD ₁₇	I/O
32	GND		72	PWRIN		112	P3300		152	GND	
33	DCA ₂₀	O	73	GND		113	DCD ₃₁	I/O	153	DCD ₉	I/O
34	DCA ₂₁	O	74	GND		114	DCD ₂₃	I/O	154	DCD ₁	I/O
35	DCA ₂₂	O	75	TOUTP	O	115	GND		155	P3300	
36	DCA ₂₃	O	76	TOUTN	O	116	DCD ₁₅	I/O	156	DCD ₂₄	I/O
37	GND		77	GND		117	DCD ₇	I/O	157	DCD ₁₆	I/O
38	DCA ₂₄	O	78	GND		118	P3300		158	$\overline{\text{DCRST}}^*$	O
39	DCA ₂₅	O	79	DCAD	I	119	DCD ₃₀	I/O	159	DCD ₈	I/O
40	P3300		80	GND		120	DCD ₂₂	I/O	160	DCD ₀	I/O

* On the Itsy mother-board version 1.1, pin 158 is connected to ground (GND).

Table 4: Daughter-card connector (j2) pin-out.

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analysis, beyond the scope of this document, is required to accommodate daughter-cards that require more current.

PWRIN: power input

3 pins are used to carry the unregulated battery voltage V_{pwrin} (see Section 2.2). The amount of current available to daughter-cards varies depending on the processing state of the Itsy computer (i.e., CPU core frequency, enabled/disabled state of all units, etc.).

$\overline{\text{DCRST}}$: daughter-card reset

On the Itsy mother-board version 1.5, this output signal is asserted (0) during a hardware reset (i.e., power-up or push-button reset). It corresponds to the input signal $\overline{\text{RESET}}$ of the StrongARM SA-1100 processor (u06) [DEC98b] buffered by an SN74LVCH16244ADGG driver (u14) [TI97a] (see Section 2.3).¹⁰

$\overline{\text{RESET_OUT}}$: reset output

This output signal is asserted (0) during a reset (i.e., hardware, software, or watch-dog reset) and during sleep mode. It is directly connected to the corresponding pin of the StrongARM SA-1100 processor (u06) [DEC98b].

PWR_EN: power enable

This output signal is asserted (1) during run mode or idle mode and de-asserted (0) during sleep mode. It is connected directly to the corresponding pin of the StrongARM SA-1100 processor (u06) [DEC98b].

$\overline{\text{DCBOOT}}$: daughter-card boot select

This input signal defines whether a daughter-card is bootable or not. It is sampled after a hardware reset (i.e., power-up or push-button reset) or while exiting sleep mode. If, at sampling time, this signal is asserted (0) and the signal GPIO₁₉ (DCEN) is set to 1, static-memory bank 0 mirrors bank 2 and the StrongARM SA-1100 processor (u06) [DEC98b] boots from the daughter-card. Otherwise, static-memory bank 0 mirrors bank 1 and the processor boots from the mother-board. A pull-up resistor keeps this signal de-asserted (1) by default. After a hardware reset, the boot memory is solely selected by the signal $\overline{\text{DCBOOT}}$, since the value of the signal GPIO₁₉ (DCEN) is always 1 (see Section 3.2). The signal $\overline{\text{DCBOOT}}$ is not sampled after a software or watch-dog reset, because the processor does not sample the signal ROM_SEL after these types of reset.¹¹

DCROMSEL: daughter-card boot ROM width select

This input signal defines the width of static-memory bank 2 on a bootable daughter-card. A value of 0 corresponds to a 16-bit bank, while a value of 1 corresponds to a 32-bit bank. A pull-up resistor sets the default value of this signal to 1. This signal is used to set the signal

¹⁰On the Itsy mother-board version 1.1, the signal $\overline{\text{DCRST}}$ does not exist and pin 158 is connected to ground (GND).

¹¹On the Itsy mother-board version 1.1, the signal $\overline{\text{DCBOOT}}$ is also sampled after a software or watch-dog reset, hence, leading to potential problems when using a 16-bit daughter-card and allowing the value of the signal $\overline{\text{DCBOOT}}$ to change.

The Itsy Pocket Computer Version 1.5: Hardware Description

ROM_SEL of the StrongARM SA-1100 processor (u06) [DEC98b] when static-memory bank 0 mirrors bank 2 (see signal $\overline{\text{DCBOOT}}$ above).

$\overline{\text{DCCS}}_{3..2}$: daughter-card static-memory chip select

These output signals control the accesses to the static-memory banks 2 and 3. The signal $\overline{\text{DCCS}}_2$ is generated directly by the PZ3032-8BC PLD (u08a) [Phi97a] and is asserted when the signal $\overline{\text{CS}}_2$ of the StrongARM SA-1100 processor (u06) [DEC98b] is asserted or when the signal $\overline{\text{CS}}_0$ is asserted and static-memory bank 0 mirrors bank 2 (see signal $\overline{\text{DCBOOT}}$ above). This signal is enabled when the signal GPIO₁₉ (DCEN) is set to 1 and disabled when it is set to 0 (see Section 3.2). The signal $\overline{\text{DCCS}}_3$ corresponds to the signal $\overline{\text{CS}}_3$ buffered by an SN74LVCH16244ADGG driver (u13) [TI97a].

$\overline{\text{DCRAS}}_{3..1}$: daughter-card DRAM row-address strobe

$\overline{\text{DCCAS}}_{3..0}$: daughter-card DRAM column-address strobe

These output signals control the accesses to the DRAM banks 1, 2, and 3. They correspond to the signals $\overline{\text{RAS}}_{3..1}$ and $\overline{\text{CAS}}_{3..0}$ of the StrongARM SA-1100 processor (u06) [DEC98b] buffered by an SN74LVCH16244ADGG driver (u13) [TI97a].

$\overline{\text{DCOE}}$: daughter-card static-memory and DRAM output enable

$\overline{\text{DCWE}}$: daughter-card static-memory and DRAM write enable

These output signals control the accesses to the static-memory banks 2 and 3 (in conjunction with the signals $\overline{\text{DCCS}}_{3..2}$) and to the DRAM banks 1, 2, and 3 (in conjunction with the signals $\overline{\text{DCRAS}}_{3..1}$ and $\overline{\text{DCCAS}}_{3..0}$). They correspond to the signals $\overline{\text{OE}}$ and $\overline{\text{WE}}$ of the StrongARM SA-1100 processor (u06) [DEC98b] buffered by an SN74LVCH16244ADGG driver (u13) [TI97a].

$\overline{\text{DCPSKTSEL}}$: daughter-card PCMCIA socket select

$\overline{\text{DCPREG}}$: daughter-card PCMCIA register select

$\overline{\text{DCPCE}}_{2..1}$: daughter-card PCMCIA chip enable

$\overline{\text{DCPOE}}$: daughter-card PCMCIA output enable

$\overline{\text{DCPWE}}$: daughter-card PCMCIA write enable

$\overline{\text{DCPIOR}}$: daughter-card PCMCIA input/output read strobe

$\overline{\text{DCPIOW}}$: daughter-card PCMCIA input/output write strobe

These output signals control the accesses to the PCMCIA interface. They correspond to the signals PSKTSEL, PREG, PCE_{2..1}, POE, PWE, PIOR, and PIOW of the StrongARM SA-1100 processor (u06) [DEC98b] buffered by SN74LVCH16244ADGG drivers (u13 and u15) [TI97a].

$\overline{\text{DCIOIS16}}$: daughter-card PCMCIA input/output is 16-bit wide

$\overline{\text{DCPWAIT}}$: daughter-card PCMCIA wait

These input signals provide feed-back from the PCMCIA interface. They correspond to the signals $\overline{\text{IOIS16}}$ and $\overline{\text{PWAIT}}$ of the StrongARM SA-1100 processor (u06) [DEC98b] buffered by an SN74LVCH16244ADGG driver (u15) [TI97a]. Pull-up resistors keep the signals $\overline{\text{IOIS16}}$ and $\overline{\text{PWAIT}}$ de-asserted (1) when the driver is disabled. It is also possible to keep the signals $\overline{\text{DCIOIS16}}$ and $\overline{\text{DCPWAIT}}$ de-asserted (1), by replacing the $\infty \Omega$ resistors r32 and r33 with pull-up resistors.

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DCA_{25..0}: daughter-card address

These output signals implement the daughter-card address bus. They correspond to the address bus A_{25..0} of the StrongARM SA-1100 processor (u06) [DEC98b] buffered by two SN74LVCH16244ADGG drivers (u14 and u15) [TI97a].

DCD_{31..0}: daughter-card data

These bi-directional signals implement the daughter-card data bus. They correspond to the data bus D_{31..0} of the StrongARM SA-1100 processor (u06) [DEC98b] buffered by two SN74LVCH16245ADGG transceivers (u16 and u17) [TI97b].

UDCP: USB device controller positive data

UDCN: USB device controller negative data

These bi-directional signals implement the USB interface. They are directly connected to the UDC+ and UDC− pins of the StrongARM SA-1100 processor (u06) [DEC98b]. No protection circuitry is provided.

RXD_1: receive data, serial port 1

TXD_1: transmit data, serial port 1

These bi-directional signals can be used to implement the SDLC or UART engine of serial port 1 or can be configured as general-purpose input/output signals, as shown in Table 5. They are directly connected to the corresponding pins of the StrongARM SA-1100 processor (u06) [DEC98b].

GPIO_{27..25,18..10,1}: general-purpose input/output

These bi-directional signals can be used as general-purpose input/output signals, as interrupts, or to implement their *alternate function*, as shown in Table 5. They are directly connected to the corresponding pins of the StrongARM SA-1100 processor (u06) [DEC98b]. It should be noted that the signal GPIO₁ can be used to wake up the processor after a hardware transition to sleep mode due to the assertion of the signal BATT_FAULT or the signal VDD_FAULT (see Section 2.2.1).

TINP: telecommunication input positive data

TINN: telecommunication input negative data

TOUTP: telecommunication output positive data

TOUTN: telecommunication output negative data

These input and output signals implement the telecommunication codec (i.e., for software modem). They are directly connected to the corresponding pins of the UCB1200 analog interface (u18) [Phi97b].

DCAD: daughter-card general-purpose analog-to-digital input

This signal is a general-purpose analog input (10-bit analog-to-digital converter, nominal voltage range: [0 V .. 7.5 V]). It is directly connected to the AD₃ pin of the UCB1200 analog interface (u18) [Phi97b].

Daughter-cards are intended to form or replace the back of an Itsy computer. Systems with only a small number of thin components can be entirely packaged on the top side of the daughter-card

The Itsy Pocket Computer Version 1.5: Hardware Description

Signal	Main/alternate function		Gen.-purp. signal		
	Function	Dir.	Dir.	Int.	Sleep
RXD_1	Serial port 1 SDLC/UART receive data	I	I/O	N	Z, 0
TXD_1	Serial port 1 SDLC/UART transmit data	O	I/O	N	Z, 0
GPIO ₁			I/O	Y	Z, 0, 1
GPIO ₁₀	Serial port 4 SSP transmit data	O	I/O	Y	Z, 0, 1
GPIO ₁₁	Serial port 4 SSP receive data	I	I/O	Y	Z, 0, 1
GPIO ₁₂	Serial port 4 SSP sample clock	O	I/O	Y	Z, 0, 1
GPIO ₁₃	Serial port 4 SSP sample frame	O	I/O	Y	Z, 0, 1
GPIO ₁₄	Serial port 1 UART transmit data	O	I/O	Y	Z, 0, 1
GPIO ₁₅	Serial port 1 UART receive data	I	I/O	Y	Z, 0, 1
GPIO ₁₆	Serial port 1 SDLC sample clock	I/O	I/O	Y	Z, 0, 1
GPIO ₁₇	Serial port 1 SDLC abort after frame	O	I/O	Y	Z, 0, 1
GPIO ₁₈	Serial port 1 UART sample clock	I	I/O	Y	Z, 0, 1
GPIO ₂₅	1 Hz clock	O	I/O	Y	Z, 0, 1
GPIO ₂₆	Internal clock ($\frac{1}{2}$ CPU core frequency)	O	I/O	Y	Z, 0, 1
GPIO ₂₇	32.768 kHz clock	O	I/O	Y	Z, 0, 1

Table 5: Daughter-card general-purpose input/output signals. The “sleep” column describes the possible sleep-mode states, the symbol “Z” means that the corresponding pin is configured as input.

PCB and, hence, fit in entirely in the case. On the other hand, systems that require more space can grow arbitrarily large on the bottom side of the daughter-card PCB. By sanding off the thin lip on the rear of the case, it is also possible to design daughter-card PCBs that are larger than the case. The mechanical specifications of daughter-cards is provided in Appendix A.

2.7.1 Static-memory identification scheme

To allow self-configuration, the software should be able to determine if a daughter-card is used or not and, if present, it should be able to recognize the daughter-card. A few resources available on the daughter-card (e.g., the DRAM banks) can be detected without any additional hardware, but this is not the case for most devices. Moreover, it is sometimes useful to only partially assemble a daughter-card (e.g., on a memory-extension daughter-card, only some of the available static-memory or DRAM banks may be present). In order to merge these requirements with the need to recognize which flash-memory circuits are used on the mother-board (see Section 2.5.1), a static-memory identification scheme — identical for all four static-memory banks of the StrongARM SA-1100 processor (u06) [DEC98b] — has been defined. Any daughter-card, using either static-memory bank 2 or 3 or using any otherwise undetectable resources (e.g., GPIO signals), should conform to this convention.

Several criteria were considered in the design of this mechanism:

The Itsy Pocket Computer Version 1.5: Hardware Description

- This scheme should be compatible with both 16-bit and 32-bit static-memory banks. That is, the configuration software should recognize a given device without prior knowledge of its width.
- Since the processor's endianness is programmable, this scheme should be defined independently of the current endianness.
- The amount of additional hardware should be minimized.

To meet these goals, each possible static-memory device should implement an 8-bit *class identification register* CID. Since there are only 256 possible values for this register, they should be assigned parsimoniously. Therefore, each value represents a class of devices (e.g., a single value is used for any non-volatile memory). Additional information, defined on a class basis, may be implemented to discriminate between different members of a class.

The address of the CID register should be fixed and easily decodable. The first word of a bank is not a good candidate, since this is the location of the reset vector in the boot static-memory bank. The first address following the exception vectors is not a good candidate either, since this is typically the position of the *fast interrupt request (FIQ)* handler routine. Hence, the last word of a bank has been adopted as the address for the CID register.

This leads to the following convention: each static-memory device should decode a read access at address $A_{25..0} = 3\text{FFFFFFE}_{16}$, with address bit A_0 ignored on a 16-bit device and address bits $A_{1..0}$ ignored on a 32-bit device. The device should then provide the 8-bit class identification value CID on the data bits $D_{7..0}$. Partial address decoding (or even no decoding) may be used as appropriate.¹²

The class identification value $\text{CID} = 255 = \text{FF}_{16}$ is reserved and will not be assigned to any static-memory device. With this knowledge, the configuration software can detect the absence of any device on a given bank, by driving the value $255 = \text{FF}_{16}$ on the data bits $D_{7..0}$ before reading the bank's CID register (the hardware is designed such that the last value driven on the data bus is preserved in the absence of any device driving the bus).

The class identification value $\text{CID} = 0$ is assigned to any non-volatile memory, that is, *read-only memory (ROM)* or flash memory.¹³ Additional information for this class is defined in Section 3.3. The CID register as well as all additional information can be simply programmed in the non-volatile memory. On many daughter-cards, it may be useful to implement a non-volatile memory for general use in addition to some other hardware (e.g., serial interface, sensors). In order to generalize the configuration software, any such static-memory device should be assigned a class identification value $\text{CID} \leq 127 = 7\text{F}_{16}$ (i.e., $\text{CID}_7 = 0$) while any other device should have a class identification value $\text{CID} > 128 = 80_{16}$ (i.e., $\text{CID}_7 = 1$). Devices of the first category should implement the same additional information as non-volatile memories with the class identification value $\text{CID} = 0$ (see Section 3.3).

¹²Although only the 26 least significant address bits $A_{25..0}$ are available on the pins of the StrongARM SA-1100 processor (u06), a 128 Mbyte address space is internally allocated to each static-memory bank. Therefore, the offset of the CID register within the static-memory bank is a 27-bit value with address bit A_{26} being ignored.

¹³For the purpose of the configuration software, it is only useful to distinguish whether a non-volatile memory can be programmed in-circuit or not. Therefore, *programmable ROM (PROM)* and *erasable programmable ROM (EPROM)* are lumped in the ROM category. Likewise, *electrically-erasable programmable ROM (EEPROM)* are lumped in the flash-memory category.

The mother-board flash memory, implemented as static-memory bank 1, conforms to the same identification scheme, with the class identification value $CID = 0$. Daughter-cards using static-memory banks 2 and 3 should implement both CID registers. Daughter-cards that do not use any static-memory bank but use other resources should dedicate one or both banks to the identification scheme. In this case, the CID register could easily be implemented using an 8-bit buffer.

3 Programmer's model

This section presents additional information on the model that the low-level software has of the Itsy hardware.

3.1 Memory map

The internal decoding of the StrongARM SA-1100 processor (u06) [DEC98b] provides a general template as how the address space is used. Table 6 shows the memory map implemented by the Itsy computer. The first column give the address range at which a particular device is decoded. The “location” column specifies whether this device is internal to the processor, is implemented on the mother-board, or whether its interface is available to the daughter-card interface. Finally, the last two columns give the device's width and size (or possible widths and sizes, when several different devices can be implemented).

As mentioned in Section 2.5, static-memory bank 0 — from which the processor boots — mirrors either bank 1 or bank 2 (see Sections 2.4, 2.7, and 3.2).

All DRAM banks must have 2^{12} rows, as imposed by DRAM bank 0 (see Section 2.5.2). This limits the size of banks 1, 2, and 3 to 16 Mbyte maximum (i.e., the largest size supported by the processor without external hardware). Using different DRAM circuits, 4 Mbyte and 8 Mbyte banks can also be implemented. Smaller banks can be considered as well. However, they are mapped in a non-contiguous address space.

3.2 Mother-board general-purpose input/output signals

Table 7 shows the general-purpose input/output signals used on the Itsy mother-board. All input signals can be used as interrupts. After a hardware reset (i.e., power-up or push-button reset), all input/output signals are configured as input. Therefore, pull-up and pull-down resistors are used to provide a default value for all signals meant to be configured as output, as shown in the last column of Table 7. The function of all signals are:

GPIO₀: \overline{MAINPB} : Main push-button

This input signal is connected to the main push-button (s02) of the Itsy computer (see Section 2.6.5). It is set to 0 when the push-button is pressed and to 1 when the push-button is released. Although this is, otherwise, a general-purpose push-button, it can be used to wake up the processor after a hardware transition to sleep mode due to the assertion of the signal BATT_FAULT or the signal VDD_FAULT (see Section 2.2.1).

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Address range	Location	Device	Width [bit]	Size
00000000 ₁₆ 07FFFFFF ₁₆		Static-memory bank 0 mirror of bank 1 or 2 (boot memory)		
08000000 ₁₆ 0FFFFFFF ₁₆	Mother-board	Static-memory bank 1 flash memory	32	4 Mbyte (max.)
10000000 ₁₆ 17FFFFFF ₁₆	Daughter-card	Static-memory bank 2	16/32	64 Mbyte (max.)
18000000 ₁₆ 1FFFFFFF ₁₆	Daughter-card	Static-memory bank 3	16/32	64 Mbyte (max.)
20000000 ₁₆ 3FFFFFFF ₁₆	Daughter-card	PCMCIA interface [DEC98b]	8/16/32	
40000000 ₁₆ 7FFFFFFF ₁₆	Reserved			
80000000 ₁₆ BFFFFFFF ₁₆	Processor (internal)	StrongARM SA-1100 registers [DEC98b]	32	
C0000000 ₁₆ C7FFFFFF ₁₆	Mother-board	DRAM bank 0	32	16 Mbyte
C8000000 ₁₆ CFFFFFFF ₁₆	Daughter-card	DRAM bank 1	32	16 Mbyte (max.)
D0000000 ₁₆ D7FFFFFF ₁₆	Daughter-card	DRAM bank 2	32	16 Mbyte (max.)
D8000000 ₁₆ DFFFFFFF ₁₆	Daughter-card	DRAM bank 3	32	16 Mbyte (max.)
E0000000 ₁₆ E7FFFFFF ₁₆	Processor (internal)	Zero bank (read only) [DEC98b]	32	128 Mbyte
E8000000 ₁₆ FFFFFFF ₁₆	Reserved			

Table 6: Memory map.

GPIO₂: PWROK: Power OK

This input signal is set to 1 during normal operation and toggles to 0 if the main power-supply voltage V_{dd} drops below the threshold $V_{dd,low}$ (i.e., $V_{dd} \leq V_{dd,low} \approx 3.0\text{ V}$), given in Table 1 (see Section 2.2.1).

GPIO₃: FLFOFF: Flash memory force off

This output signal is used to control the reset/power-down pin of the flash-memory circuits (see Section 2.5.1). When this signal is set to 0, the reset/power-down pins are asserted (0). When it is set to 1, the reset/power-down pins are only asserted (0) during a reset (i.e., hardware, software, or watch-dog reset) and during sleep mode. A pull-up resistor sets the default value of this signal to 1 when the GPIO₃ pin is configured as input (e.g., after a

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Signal	Name	Function	Dir.	Def.
GPIO ₀	MAINPB	Main push-button	I	
GPIO ₂	PWROK	Power OK	I	
GPIO ₃	FLFOFF	Flash memory force off	O	1
GPIO ₄	FL0RY/ $\overline{\text{BY}}$	Flash memory 0 ready/busy	I	
GPIO ₅	FL1RY/ $\overline{\text{BY}}$	Flash memory 1 ready/busy	I	
GPIO ₆	CODECINT	Codec interrupt	I	
GPIO ₇	UARTVALID	UART receive signal valid	I	
GPIO ₈	UARTDSR	UART data set ready	I	
GPIO ₉	UARTDTR	UART data terminal ready	O	0
GPIO ₁₉	DCEN	Daughter-card enable	O	1
GPIO ₂₀	LCDEN	LCD enable	O	0
GPIO ₂₁	AUXLCDEN	Auxiliary LCD controller enable	O	0
GPIO ₂₂	IRDAEN	IrDA transceiver enable	O	1
GPIO ₂₃	UARTFOFF	UART force off	O	0
GPIO ₂₄	UARTFON	UART force on	O	0

Table 7: Mother-board general-purpose input/output signals.

hardware reset). When the Itsy computer must boot from the mother-board, this signal should never be set to 0 during sleep mode, since the processor would be unable to read the boot memory upon wake up. This can be easily achieved by setting bit 3 of the *power manager GPIO sleep state register* PGSR of the StrongARM SA-1100 processor (u06) [DEC98b] to 1.

GPIO₄: FL0RY/ $\overline{\text{BY}}$: **Flash** memory **0** ready/busy

This input signal is connected to the ready/not-busy pin of the flash-memory circuit used for the least significant 16 data bits D_{15..0} (see Section 2.5.1). It is set to 0 when the flash-memory circuit is executing an erase or program operation and to 1 when it is ready for use.

GPIO₅: FL1RY/ $\overline{\text{BY}}$: **Flash** memory **1** ready/busy

This input signal is connected to the ready/not-busy pin of the flash-memory circuit used for the most significant 16 data bits D_{31..16} (see Section 2.5.1). It is set to 0 when the flash-memory circuit is executing an erase or program operation and to 1 when it is ready for use.

GPIO₆: CODECINT: **Codec** interrupt

This input signal is connected to the interrupt pin IRQOUT of the UCB1200 analog interface (u18) [Phi97b]. It is set to 1 when an interrupt is pending and to 0 otherwise.

GPIO₇: UARTVALID: **UART** receive signal **valid**

This input signal is connected to the $\overline{\text{INVALID}}$ pin of the MAX3223CAP RS-232 driver (u20)

[Max96], used with the UART engine of serial port 3 (see Section 2.6.3). It is set to 1 when a valid RS-232 input signal is detected (i.e., the serial interface is connected to a powered system) and to 0 when no valid signals are detected (i.e., the serial interface is unconnected or is connected to a unpowered system).

GPIO₈: UARTDSR: UART data set ready

This input signal is connected to the second receive buffer pin R2OUT of the MAX3223CAP RS-232 driver (u20) [Max96], used with the UART engine of serial port 3 (see Section 2.6.3). It can be used by software to monitor one of the RS-232 incoming signals, for example, the *data set ready* signal DSR. The exact signal that is monitored is determined by the serial-interface cable used.

GPIO₉: UARTDTR: UART data terminal ready

This output signal is connected to the second transmit buffer of the MAX3223CAP RS-232 driver (u20) [Max96], used with the UART engine of serial port 3 (see Section 2.6.3). A pull-down resistor sets the default value of this signal to 0 when the GPIO₉ pin is configured as input (e.g., after a hardware reset). It can be used by software to emulate one of the RS-232 outgoing signals, for example, the *data terminal ready* signal DTR. The exact signal that is emulated is determined by the serial-interface cable used.

GPIO₁₉: DCEN: Daughter-card enable

This output signal is used to control the SN74LVCH16244ADGG drivers (u13, u14, and u15) [TI97a] and the SN74LVCH16245ADGG transceivers (u16 and u17) [TI97b] used to buffer some daughter-card signals (see Section 2.7). These buffers are enabled when this signal is set to 1 and disabled when it is set to 0. A pull-up resistor sets the default value of this signal to 1 when the GPIO₁₉ pin is configured as input (e.g., after a hardware reset). When the Itsy computer should boot from the daughter-card, this signal should not be set to 0 during sleep mode, since the processor would be unable to access the daughter-card upon wake up. This can be easily achieved by setting bit 19 of the *power manager GPIO sleep state register* PGSR of the StrongARM SA-1100 processor (u06) [DEC98b] to 1. On the other hand, this signal can be de-asserted (0) during sleep mode, in order to force the processor to boot from the mother-board even if a bootable daughter-card is present (see Sections 2.4 and 2.7).

GPIO₂₀: LCDEN: LCD enable

This output signal is connected to the enable pins $\overline{\text{DOFF1}}$ and $\overline{\text{DOFF2}}$ of the TCM-A0822-xx LCD [Eps97] (see Section 2.6.1). The LCD is enabled when this signal is set to 1 and disabled when it is set to 0. A pull-down resistor sets the default value of this signal to 0 when the GPIO₂₀ pin is configured as input (e.g., after a hardware reset).

GPIO₂₁: AUXLCDEN: Auxiliary LCD controller enable

This output signal is used to control the auxiliary LCD controller (see Sections 2.4 and 2.6.1). The auxiliary LCD controller is enabled when this signal is set to 1 and disabled when it is set to 0. A pull-down resistor sets the default value of this signal to 0 when the GPIO₂₁ pin is configured as input (e.g., after a hardware reset). A black-and-white image (no grey levels) is captured at the first end-of-frame that the value of this signal is 1 and remains displayed as

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long as this signal and the signal GPIO_{20} (LCDEN) both stay at 1, even when the processor is in sleep mode.

GPIO_{22} : $\overline{\text{IRDAEN}}$: IrDA transceiver enable

This output signal is connected to the $\overline{\text{SD}}$ pin (shown as $\overline{\text{PD}}$ on the schematics) of the MiniSIR2 IrDA transceiver (u19) [Nov98] (see Section 2.6.4). The transceiver is enabled when this signal is set to 0 and disabled when it is set to 1. A pull-up resistor sets the default value of this signal to 1 when the GPIO_{22} pin is configured as input (e.g., after a hardware reset).

GPIO_{23} : $\overline{\text{UARTFOFF}}$: UART force off

This output signal is connected to the control pin $\overline{\text{FORCEOFF}}$ of the MAX3223CAP RS-232 driver (u20) [Max96], used with the UART engine of serial port 3 (see Section 2.6.3). When this signal is set to 0, the driver is disabled. When it is set to 1, the driver is either enabled or in AutoShutdown mode, depending on the value of the signal GPIO_{24} (UARTFON). A pull-down resistor sets the default value of this signal to 0 when the GPIO_{23} pin is configured as input (e.g., after a hardware reset).

GPIO_{24} : UARTFON: UART force on

This output signal is connected to the control pin FORCEON of the MAX3223CAP RS-232 driver (u20) [Max96], used with the UART engine of serial port 3 (see Section 2.6.3). When the signal GPIO_{23} ($\overline{\text{UARTFOFF}}$) is set to 0, this signal has no effect. Otherwise, the driver is enabled when this signal is set to 1 and is in AutoShutdown mode when it is set to 0. A pull-down resistor sets the default value of this signal to 0 when the GPIO_{24} pin is configured as input (e.g., after a hardware reset). In AutoShutdown mode, the driver is only enabled when a valid RS-232 input signal is detected (i.e., the serial interface is connected to a powered system) and is disabled when no valid signals are detected (i.e., the serial interface is unconnected or is connected to a unpowered system). When the driver is disabled in AutoShutdown mode, transmitting data will not enable it. As a consequence, a potential dead-lock might happen when the serial interface is connected to another similar interface (e.g., when two Itsy computers are connected together), since both drivers might remain disabled. To avoid this, the software should briefly set this signal to 1 when establishing a connection. The driver can then be switched to AutoShutdown mode by toggling this signal to 0.

3.3 Non-volatile memory identification structure

As mentioned in Section 2.7.1, the class identification value $\text{CID} = 0$ is assigned to any non-volatile memory (i.e., ROM or flash memory). Moreover, any daughter-card that include a non-volatile memory in addition to some other hardware should be assigned a class identification value $\text{CID} \leq 127 = 7\text{F}_{16}$ (i.e., $\text{CID}_7 = 0$). All these devices must implement the *non-volatile memory identification structure* in the last 32 bytes of the non-volatile memory.

In addition to the class identification value CID, these devices must provide the following information on the data bits $\text{D}_{15..0}$, when a read access is decoded at address $\text{A}_{25..0} = 3\text{FFFFFFE}_{16}$ (with

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address bit A_0 ignored on a 16-bit devices and address bits $A_{1..0}$ ignored on a 32-bit devices):

$A_{25..0}$	15	11	10	9	8	7	0
$3FFFFFFE_{16}$	SIZE	W	D	R	CID $\leq 127 = 7F_{16}$		

Where the additional fields have the following meaning:

R: Read-only static memory

A value of 0 indicates a flash memory, while a value of 1 indicates a ROM.

D: Daughter-card static memory

A value of 0 indicates a non-volatile memory on the mother-board, while a value of 1 indicates a non-volatile memory on a daughter-card. This bit should be set to 0 for static-memory bank 1 and to 1 for banks 2 and 3. It can be used to determine whether bank 0 mirrors bank 1 or bank 2 (see Sections 2.4, 2.7, and 3.2).

W: Static-memory width

A value of 0 indicates a 32 bit non-volatile memory, while a value of 1 indicates a 16 bit non-volatile memory.

SIZE: Base-2 logarithm of static-memory size

This field provides the logarithm in base 2 of the non-volatile memory's size, expressed in bytes.

The rest of the non-volatile memory identification structure contains the initialization values of the *static memory control register* MSC0 or MSC1 of the StrongARM SA-1100 processor (u06) [DEC98b], for all possible clock frequencies, as well as the information about which general-purpose input/output signals are associated with the non-volatile memory (if any). Figures 6 and 7 show this structure for 16-bit and 32-bit devices respectively. The initialization software should copy the MSC value for the current CPU frequency f_{cpu} into the appropriate field of the MSC0 or MSC1 register. The fields defining the general-purpose input/output signals have the following meaning:

EN0: Static-memory enable 0

This field provides the number of the output GPIO pin (if any) used to enable or disable the least significant 16 bits ($D_{15..0}$) of the non-volatile memory. When no such pin is used, this field should be set to the special value $EN0 = 255 = FF_{16}$. The non-volatile memory should be enabled when this pin is set to 1 and disabled when it is set to 0.

RY/ \overline{BY} 0: Static-memory ready/busy 0

This field provides the number of the input GPIO pin (if any) used to monitor the ready or busy state of the least significant 16 bits ($D_{15..0}$) of the non-volatile memory (i.e., flash memory). When no such pin is used, this field should be set to the special value $RY/\overline{BY}0 = 255 = FF_{16}$. The ready state should be indicated by a value of 1 and the busy state by a value of 0.

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A _{25..0}	15	8	7	0
3FFFFE0 ₁₆	MSC ($f_{\text{cpu}} = 16 \cdot f_{\text{crystal}} = 59.0 \text{ MHz}$)			
3FFFFE2 ₁₆	MSC ($f_{\text{cpu}} = 20 \cdot f_{\text{crystal}} = 73.7 \text{ MHz}$)			
3FFFFE4 ₁₆	MSC ($f_{\text{cpu}} = 24 \cdot f_{\text{crystal}} = 88.5 \text{ MHz}$)			
3FFFFE6 ₁₆	MSC ($f_{\text{cpu}} = 28 \cdot f_{\text{crystal}} = 103.2 \text{ MHz}$)			
3FFFFE8 ₁₆	MSC ($f_{\text{cpu}} = 32 \cdot f_{\text{crystal}} = 118.0 \text{ MHz}$)			
3FFFFEA ₁₆	MSC ($f_{\text{cpu}} = 36 \cdot f_{\text{crystal}} = 132.7 \text{ MHz}$)			
3FFFFEC ₁₆	MSC ($f_{\text{cpu}} = 40 \cdot f_{\text{crystal}} = 147.5 \text{ MHz}$)			
3FFFFEE ₁₆	MSC ($f_{\text{cpu}} = 44 \cdot f_{\text{crystal}} = 162.2 \text{ MHz}$)			
3FFFFF0 ₁₆	MSC ($f_{\text{cpu}} = 48 \cdot f_{\text{crystal}} = 176.9 \text{ MHz}$)			
3FFFFF2 ₁₆	MSC ($f_{\text{cpu}} = 52 \cdot f_{\text{crystal}} = 191.7 \text{ MHz}$)			
3FFFFF4 ₁₆	MSC ($f_{\text{cpu}} = 56 \cdot f_{\text{crystal}} = 206.4 \text{ MHz}$)			
3FFFFF6 ₁₆	Reserved			
3FFFFF8 ₁₆	Reserved			
3FFFFFA ₁₆	RY/ $\overline{\text{BY}}$ 0		EN0	
3FFFFFC ₁₆	Reserved			
3FFFFFE ₁₆	SIZE	1	D R	CID $\leq 127 = 7\text{F}_{16}$

Figure 6: Non-volatile memory identification structure for 16-bit devices.

EN1: Static-memory **enable** 1

This field provides the number of the output GPIO pin (if any) used to enable or disable the most significant 16 bits (D_{31..16}) of the non-volatile memory. When no such pin is used, this field should be set to the special value EN1 = 255 = FF₁₆. The non-volatile memory should be enabled when this pin is set to 1 and disabled when it is set to 0.

RY/ $\overline{\text{BY}}$ 1: Static-memory **ready/busy** 1

This field provides the number of the input GPIO pin (if any) used to monitor the ready or busy state of the most significant 16 bits (D_{31..16}) of the non-volatile memory (i.e., flash memory). When no such pin is used, this field should be set to the special value RY/ $\overline{\text{BY}}$ 1 = 255 = FF₁₆. The ready state should be indicated by a value of 1 and the busy state by a value of 0.

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$A_{25..0}$	31	24 23	16 15	8 7	0
$3FFFFE0_{16}$	MSC ($f_{\text{cpu}} = 16 \cdot f_{\text{crystal}} = 59.0 \text{ MHz}$)		MSC ($f_{\text{cpu}} = 20 \cdot f_{\text{crystal}} = 73.7 \text{ MHz}$)		
$3FFFFE4_{16}$	MSC ($f_{\text{cpu}} = 24 \cdot f_{\text{crystal}} = 88.5 \text{ MHz}$)		MSC ($f_{\text{cpu}} = 28 \cdot f_{\text{crystal}} = 103.2 \text{ MHz}$)		
$3FFFFE8_{16}$	MSC ($f_{\text{cpu}} = 32 \cdot f_{\text{crystal}} = 118.0 \text{ MHz}$)		MSC ($f_{\text{cpu}} = 36 \cdot f_{\text{crystal}} = 132.7 \text{ MHz}$)		
$3FFFFEC_{16}$	MSC ($f_{\text{cpu}} = 40 \cdot f_{\text{crystal}} = 147.5 \text{ MHz}$)		MSC ($f_{\text{cpu}} = 44 \cdot f_{\text{crystal}} = 162.2 \text{ MHz}$)		
$3FFFFF0_{16}$	MSC ($f_{\text{cpu}} = 48 \cdot f_{\text{crystal}} = 176.9 \text{ MHz}$)		MSC ($f_{\text{cpu}} = 52 \cdot f_{\text{crystal}} = 191.7 \text{ MHz}$)		
$3FFFFF4_{16}$	MSC ($f_{\text{cpu}} = 56 \cdot f_{\text{crystal}} = 206.4 \text{ MHz}$)		Reserved		
$3FFFFF8_{16}$	RY/ $\overline{\text{BY}}1$		EN1		Reserved
$3FFFFFC_{16}$	Reserved		SIZE	0	D R CID $\leq 127 = 7F_{16}$

Figure 7: Non-volatile memory identification structure for 32-bit devices.

When a single GPIO pin is used to enable a 32 bit non-volatile memory, the EN0 and EN1 fields should both provide the same value. The same applies to the RY/ $\overline{\text{BY}}0$ and RY/ $\overline{\text{BY}}1$ fields.

For example, the address $A_{25..0} = 3FFFFF8_{16}$ of the mother-board flash memory should be set to the value $D_{31..0} = 05030403_{16}$ (see Section 3.2).

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- [Vir98] Marc A. Viredaz. *The Itsy Pocket Computer Version 1.5: User's Manual*. Technical note TN-54, WRL, Compaq, Palo Alto, CA (USA), July 1998. Revision 1.0.

A Daughter-card mechanical specifications

Figure 8 presents the mechanical specifications for daughter-cards. On the top side (i.e., connector side), no components should be placed outside the specified component keep-in area. Components whose height does not exceed 1.2 mm can be placed anywhere within the keep-in area. This rule is conservative, since higher components can be positioned in several sub-areas. However, it is beyond the scope of this document to specify these exceptions. Since the daughter-card forms the back of the Itsy computer, there are no restrictions as to where components can be placed on the bottom side.

The 3.4 mm hole is optional. Its aim is to provide an air channel to the back of the noise-canceling microphone (j7). Since this feature improves the quality of the audio input, it is highly recommended to include it on any daughter-card (unless it jeopardizes the placement and/or routing of the daughter-card).

The daughter-card connector to be used with the Itsy mother-board version 1.5 is a Nais AXK5SA6075P model.¹⁴

Figure 9 specifies the pad layout for the connector.¹⁵ The specified pad dimensions should correspond to the area available for soldering. That is, with PCB technologies using gasketed pads (i.e., the size of the solder mask openings are smaller than the size of the copper pads), the specified dimensions are for the solder mask openings, while with PCB technologies using non-gasketed pads (i.e., the size of the solder mask openings are larger than or equal to the size of the copper pads), these dimensions are those of the copper pads.

¹⁴The Itsy mother-board version 1.1 uses a different manufacturer and the mating connector to be used on its daughter-cards is a JAE WR-160PB-VF-1 model.

¹⁵This pad layout accommodates both the JAE WR-160PB-VF-1 and Nais AXK5SA6075P connectors to be used with the Itsy mother-board versions 1.1 and 1.5 respectively.

The Itsy Pocket Computer Version 1.5: Hardware Description

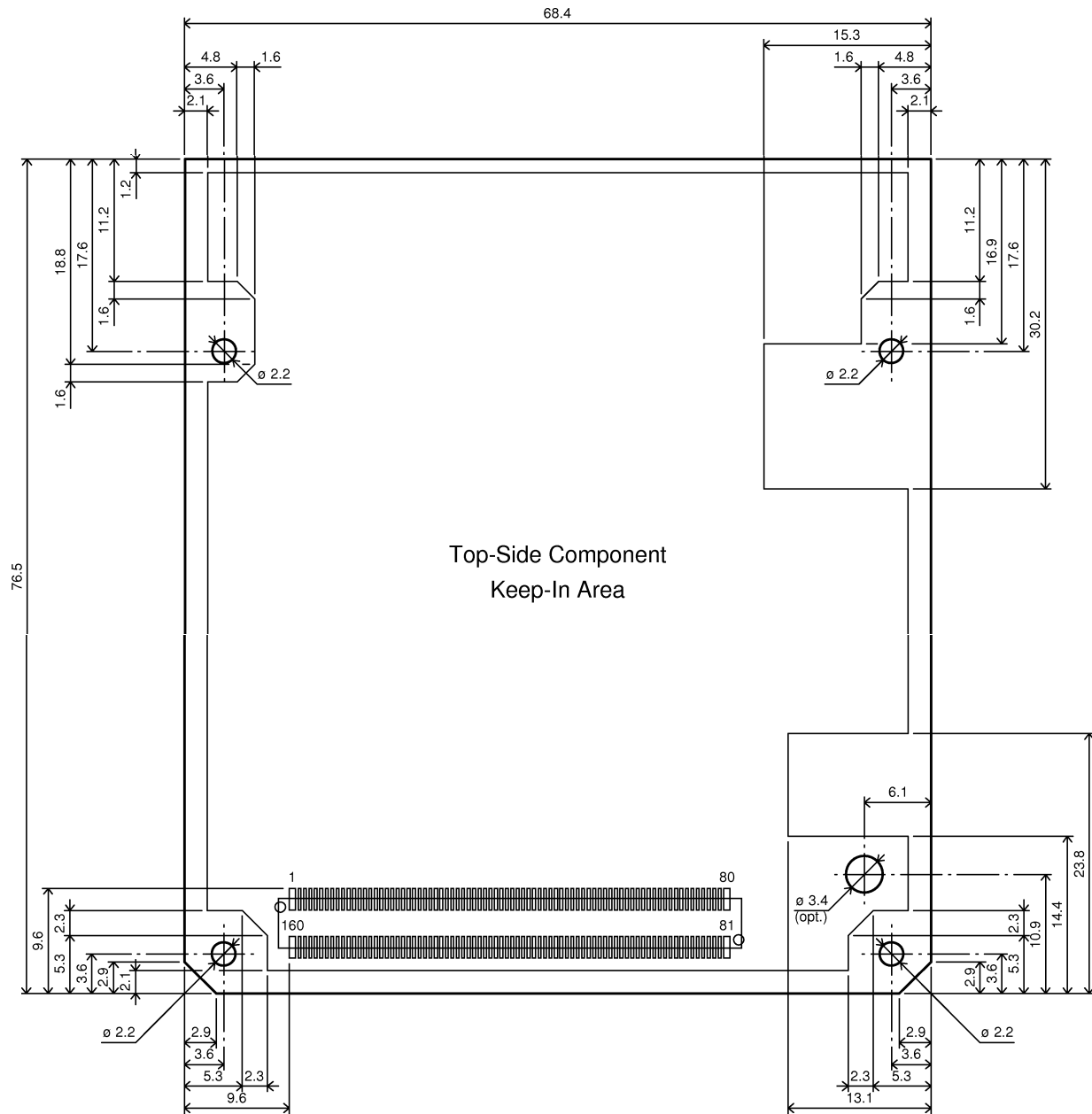
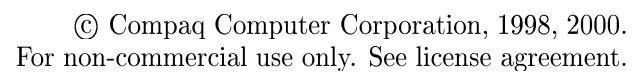


Figure 8: Daughter-card mechanical specifications (all dimensions are in millimeters).

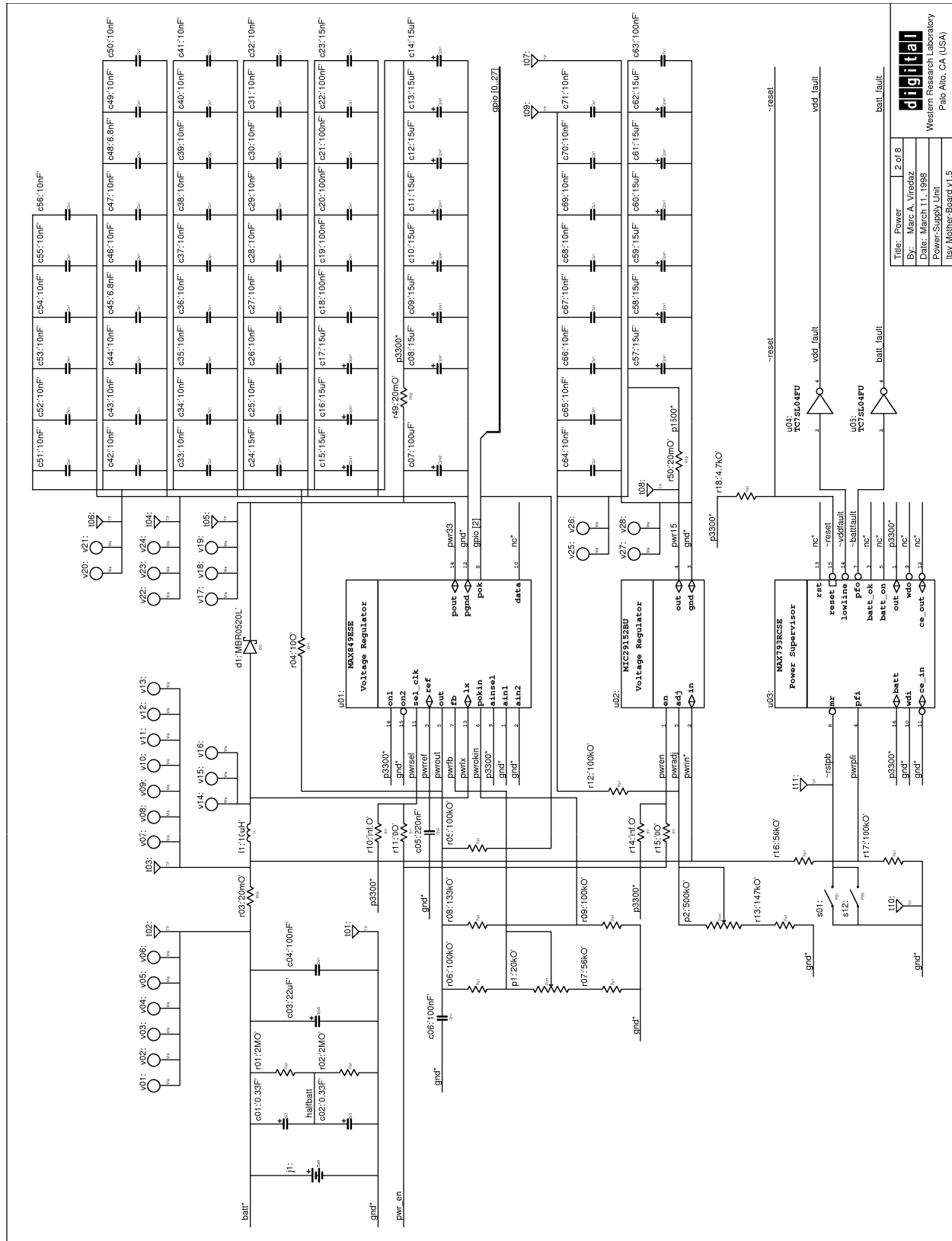
32

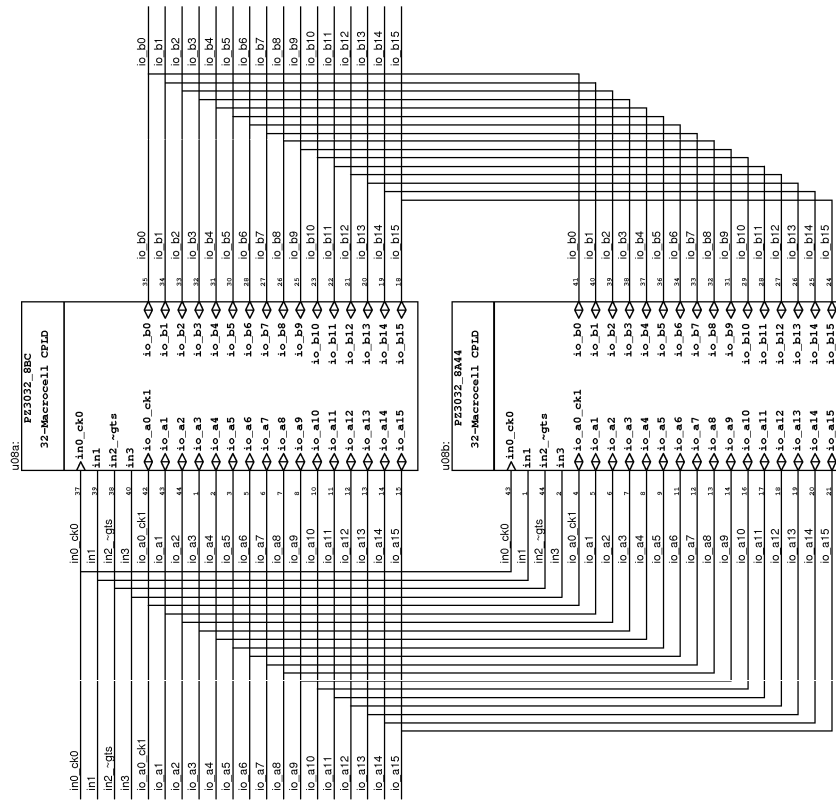


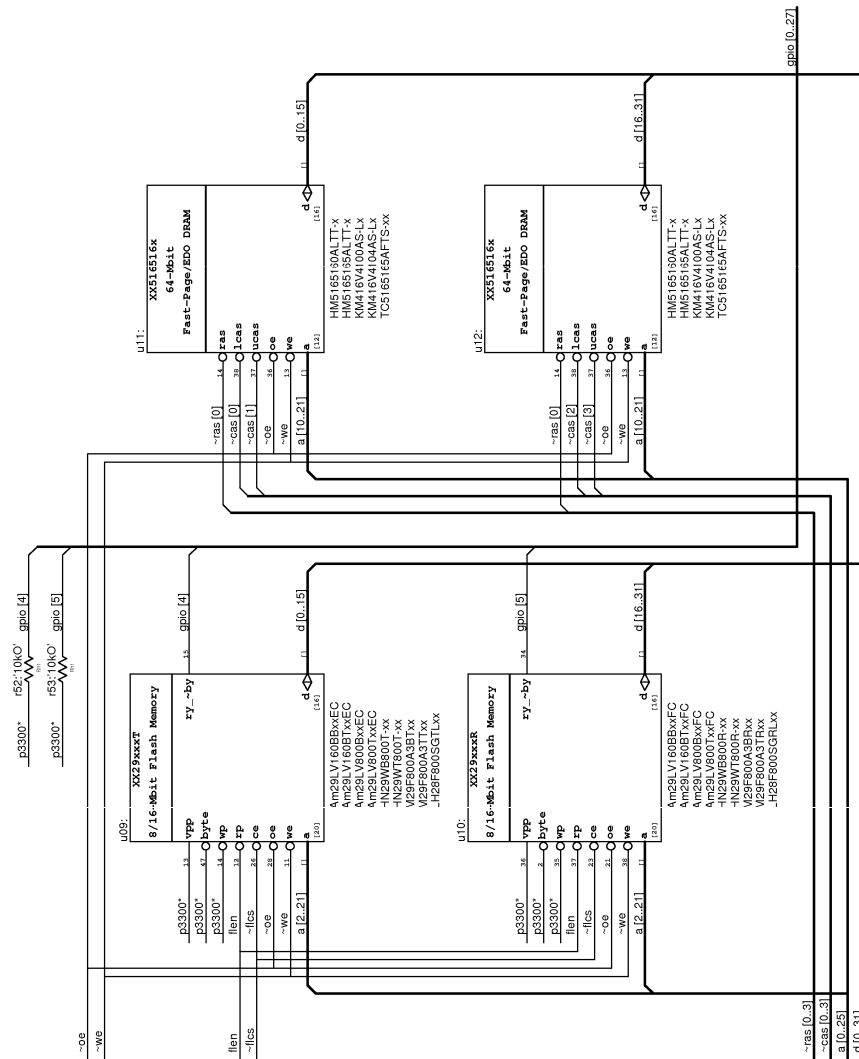
B Schematics

The following 8 pages contain the schematics of the Itsy mother-board version 1.5, drawn using the WindowSIL CAD tool [Tha97].¹⁶

¹⁶The schematics of the Itsy mother-board version 1.1 are not included.



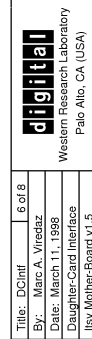


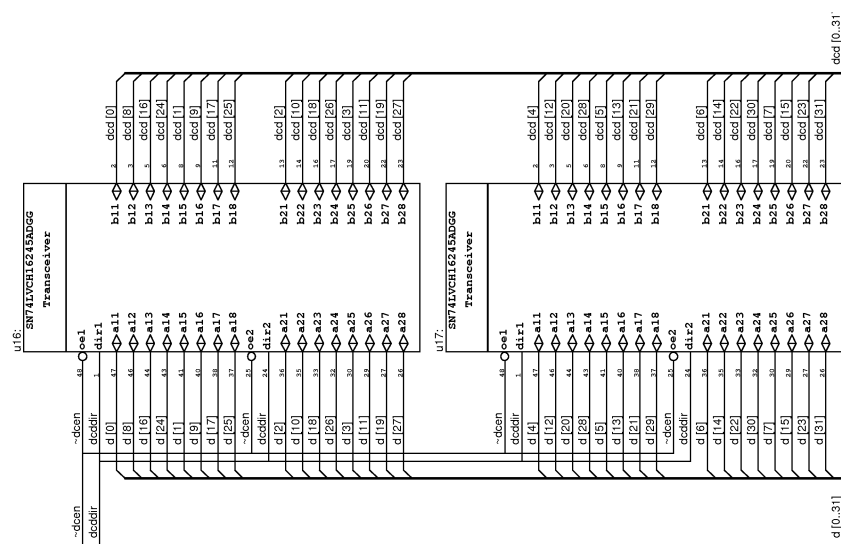


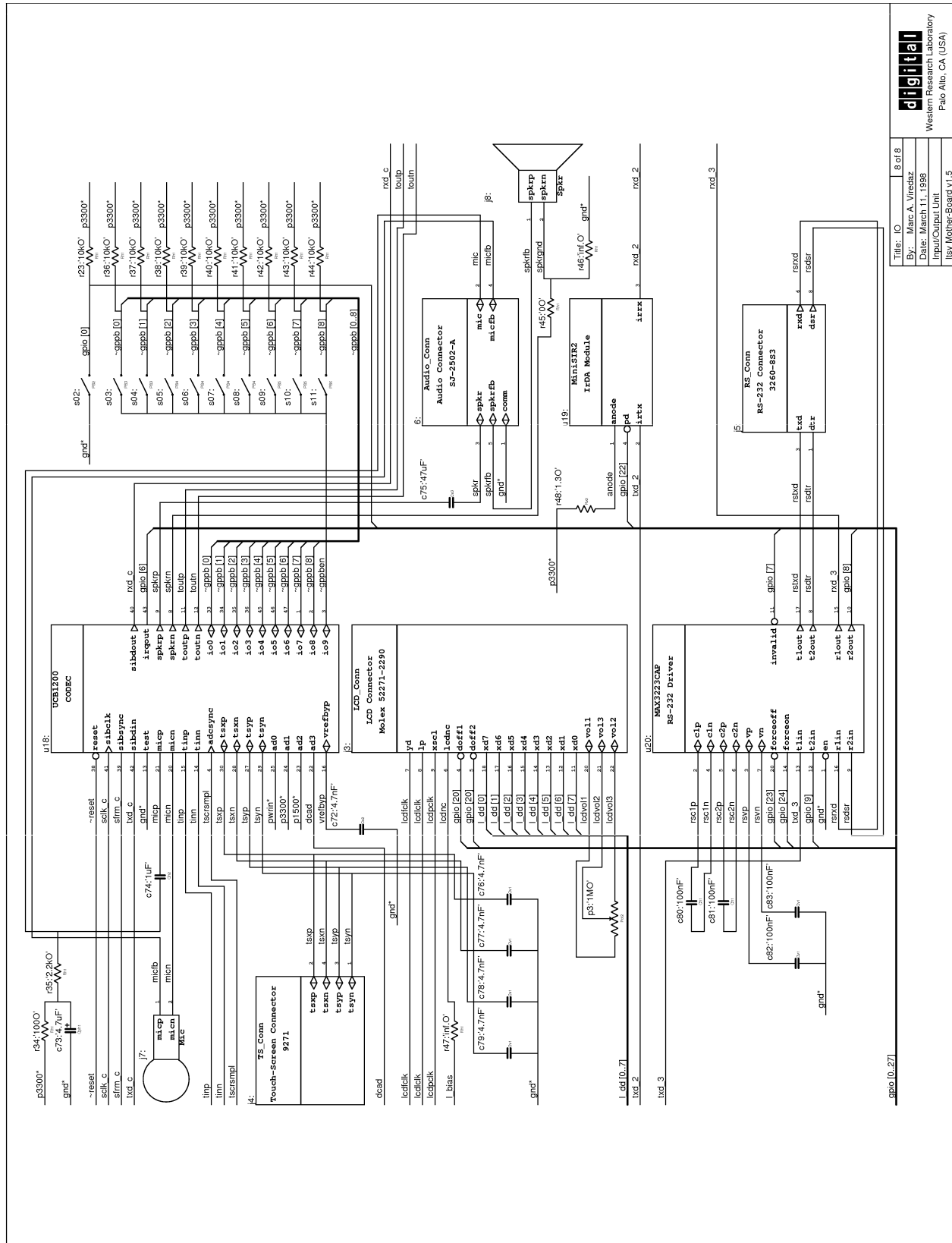
Title: Memory	5 of 8
By: Marc A. Vredaz	
Date: March 11, 1998	
Memory Unit	
lss/Mother-Board v1.5	

digital

Western Research Laboratory
Palo Alto, CA (USA)







The Itsy Pocket Computer Version 1.5: Hardware Description

C PLD listing

The following listing is the ABEL source code for the PZ3032-8BC PLD (u08a) [Phi97a] of the Itsy mother-board version 1.5.¹⁷

```
MODULE
TITLE      'IcCtrl
           'Itsy Controller'

" File      ictrl-t.abl
" Version   1.5
" Author    Marc A. Viredaz
"           DEC Western Research Laboratory, Palo Alto, CA
"           February 1998 (July 1997)
" Language  Abel
" Tool      Philips Synario, Windows 95/Windows NT
" Component Philips PZ3032-8BC
" Circuit    Itsy Mother-Board v1.5
" Function   Memory and LCD auxiliary controller.

DECLARATIONS

" Input pins

AUXCLK      PIN 37 ;          " AUXiliary CLock (1 MHz)
!RESET      PIN 43 ;          " RESET
!RESET_OUT  PIN 44 ;          " RESET Output (SA-1100)
PWR_EN      PIN 1 ;          " PoWeR ENable (SA-1100)
!CS0        PIN 2 ;          " static memory Chip Select bank [0]
!CS1        PIN 3 ;          " static memory Chip Select bank [1]
!CS2        PIN 5 ;          " static memory Chip Select bank [2]
!CS3        PIN 6 ;          " static memory Chip Select bank [3]
!RAS1       PIN 7 ;          " DRAM Row Address Strobe bank [1]
!RAS2       PIN 8 ;          " DRAM Row Address Strobe bank [2]
!RAS3       PIN 10 ;         " DRAM Row Address Strobe bank [3]
!OE         PIN 11 ;         " static memory and DRAM Output Enable
!POE        PIN 12 ;         " PCMCIA memory and attribute space
                               " Output Enable
!PIOR       PIN 13 ;         " PCMCIA I/O space Read
!DCBOOT     PIN 14 ;         " Daughter-Card BOOT select
DCROMSEL    PIN 15 ;         " Daughter-Card boot ROM width SElect
                               " (0: 16 bits, 1: 32 bits)
!FLFOFF     PIN 20 ;         " Flash memory Force OFF (GPIO [3])
DCEN_IN     PIN 19 ;         " Daughter-Card ENable INput
                               " (GPIO [19])
L_FCLK      PIN 39 ;         " LCD controller Frame CLock
L_LCLK      PIN 38 ;         " LCD controller Line CLock
L_PCLK      PIN 40 ;         " LCD controller Pixel CLock
AUXLCDEN    PIN 18 ;         " AUXiliary LCD controller ENable
                               " (GPIO [21])

" Output pins

ROM_SEL     PIN 35 ISTYPE 'com' ; " boot ROM width SElect
                               " (0: 16 bits, 1: 32 bits)
FLEN        PIN 34 ISTYPE 'com' ; " Flash memory ENable
!FLCS       PIN 33 ISTYPE 'com' ; " Flash memory Chip Select
!DCEN       PIN 32 ISTYPE 'com' ; " Daughter-Card ENable
!DCCS2      PIN 31 ISTYPE 'com' ; " Daughter-Card Chip Select bank [2]
DCDDIR      PIN 30 ISTYPE 'com' ; " Daughter-Card Data DIRection
                               " (0: read, 1: write)
LCDCLK      PIN 28 ISTYPE 'com' ; " LCD Frame CLock
LCDLCLK     PIN 27 ISTYPE 'com' ; " LCD Line CLock
LCDPCLK     PIN 26 ISTYPE 'com' ; " LCD Pixel CLock

" Buried macrocells

DC_FLBOOT   PIN 25 ISTYPE 'com,keep,retain' ;
                               " Daughter-Card/Flash memory BOOT ROM
                               " (not connected)
SREF        PIN 23 ISTYPE 'com,keep' ;
                               " DRAM Self-REFresh (not connected)
LNCNTCLK    PIN 42 ISTYPE 'com,keep' ;
                               " LCD LiNe CouNTER CLock
                               " (not connected)
FCLKDET     PIN 22 ISTYPE 'com,keep' ;
                               " LCD Frame CLock DETected (not
                               " connected)
AUXLCD1     NODE 46 ISTYPE 'reg' ; " AUXiliary LCD controller 1
AUXLCD2     PIN 21 ISTYPE 'reg' ; " AUXiliary LCD controller 2
LCLKCNT5 .. LCLKCNT0
LNCNT7 .. LNCNT0
LNCNT0      NODE 54..47 ISTYPE 'reg' ;
                               " LCD LiNe CouNTER [7:0]
                               " LCD LiNe CouNTER [7:0]

INTLCLK     NODE ISTYPE 'reg' ; " INTernal LCD Line CLock
INTFLCLK    NODE ISTYPE 'reg' ; " INTernal LCD Frame CLock

LCLKCNT     = [LCLKCNT5 .. LCLKCNT0] ;
LNCNT       = [LNCNT7 .. LNCNT0] ;

" Constants

ROMWdth     = 1 ;             " Itsy boot ROM Width
                               " (0: 16 bits, 1: 32 bits)
NbLine      = 200 ;          " Number of Lines of the LCD
LClkPer     = 55000 ;        " LCD Line CLock Period: 55000 ns
                               " (specified: 50000-125000 ns)
AuxClkPer   = 1000 ;         " Auxiliary CLock Period: 1000 ns

EQUATIONS

DC_FLBOOT   = (RESET # !PWR_EN) & DCEN_IN & DCBOOT #
               !(RESET # !PWR_EN) & DC_FLBOOT.COM #
               DCEN_IN & DCBOOT & DC_FLBOOT.COM ;

SREF        = !(PWR_EN & !RAS1 & !RAS2 & !RAS3) &
               (!PWR_EN # SREF.COM) ;

ROM_SEL     = !DC_FLBOOT.COM & ROMWdth # DC_FLBOOT.COM & DCROMSEL ;

FLEN        = !RESET_OUT & PWR_EN & !FLFOFF ;

FLCS        = !DC_FLBOOT.COM & CS0 # CS1 ;

DCEN        = DCEN_IN ;

DCCS2       = DC_FLBOOT.COM & CS0 # CS2 ;
DCCS2.OE    = DCEN_IN ;

DCDDIR      = !(OE &
               (DC_FLBOOT.COM & CS0 # CS2 # CS3 #
                RAS1 & !SREF.COM # RAS2 & !SREF.COM # RAS3 & !SREF.COM) #
               POE # PIOR) ;

LNCNTCLK    = !(AUXLCDEN & FCLKDET.COM & !L_FCLK & !AUXLCD1.FB & L_LCLK #
               AUXLCDEN & AUXLCD2.FB & INTLCLK.FB) ;

FCLKDET     = !(AUXLCDEN # RESET) & (L_FCLK # FCLKDET.COM) ;

AUXLCD1     := FCLKDET.COM & !L_FCLK & !AUXLCD1.FB &
               (LNCNT.FB == NbLine - 2) #
               AUXLCD1.FB ;
AUXLCD1.CLK = LNCNTCLK ;
AUXLCD1.ACLR = !AUXLCDEN # RESET ;

AUXLCD2     := AUXLCD1.FB ;
AUXLCD2.CLK = AUXCLK ;
AUXLCD2.ACLR = !AUXLCDEN # RESET ;

LCLKCNT     := AUXLCD2.FB & (LCLKCNT.FB < LClkPer/AuxClkPer - 1) &
               (LCLKCNT.FB + 1) ;
LCLKCNT.CLK = AUXCLK ;
LCLKCNT.ACLR = !AUXLCDEN # RESET ;

LNCNT       := (LNCNT.FB < NbLine - 1) & (LNCNT.FB + 1) ;
LNCNT.CLK   = LNCNTCLK ;
LNCNT.ACLR  = !AUXLCDEN # RESET ;

INTLCLK     := AUXLCD2.FB & (LCLKCNT.FB == LClkPer/AuxClkPer - 1) ;
INTLCLK.CLK = AUXCLK ;
INTLCLK.ACLR = !AUXLCDEN # RESET ;

INTFLCLK    := AUXLCD2.FB & (LCLKCNT.FB == LClkPer/AuxClkPer - 1) &
               (LNCNT.FB == NbLine - 1) #
               INTLCLK.FB & INTFLCLK.FB ;
INTFLCLK.CLK = AUXCLK ;
INTFLCLK.ACLR = !AUXLCDEN # RESET ;

LCDPCLK     = !AUXLCD1.FB & L_FCLK # AUXLCD2.FB & INTFLCLK.FB ;

LCDLCLK     = !AUXLCD1.FB & L_LCLK # AUXLCD2.FB & INTLCLK.FB ;

LCDPCLK     = !AUXLCD1.FB & L_PCLK ;

END ICtrl
```

¹⁷The PLD source code for the Itsy mother-board version 1.1 is not included.

D Printed-circuit board layout

Figures 10 and 11 present respectively the top-side and bottom-side PCB layout of the Itsy mother-board version 1.5, while Tables 8 and 9 show the component list sorted by component numbers and component references, respectively.¹⁸

Component					Component				
No.	Ref.	Schematic body	Value	Schematic	No.	Ref.	Schematic body	Value	Schematic
0	u16	SN74LVCH16245ADGG		DataBuf (p. 7)	55	u18	UCB1200		I/O (p. 8)
1	u17	SN74LVCH16245ADGG		DataBuf (p. 7)	56	r52	Rh1	10k0	Memory (p. 5)
2	j2	DC_Conn		DCIntf (p. 6)	57	r53	Rh1	10k0	Memory (p. 5)
3	r32	Rv1	inf.0	DCIntf (p. 6)	58	u10	XX29xxxR		Memory (p. 5)
4	r33	Rv1	inf.0	DCIntf (p. 6)	59	u09	XX29xxxT		Memory (p. 5)
5	u13	SN74LVCH16244ADGG		DCIntf (p. 6)	60	u11	XX516516x		Memory (p. 5)
6	u14	SN74LVCH16244ADGG		DCIntf (p. 6)	61	u12	XX516516x		Memory (p. 5)
7	u15	SN74LVCH16244ADGG		DCIntf (p. 6)	62	s1	Mnt		Itsy (p. 1)
8	j6	Audio_Conn		I/O (p. 8)	63	s2	Mnt		Itsy (p. 1)
9	c80	Ch1	100nF	I/O (p. 8)	64	j1	Batt		Power (p. 2)
10	c81	Ch1	100nF	I/O (p. 8)	65	c06	Ch1	100nF	Power (p. 2)
11	c74	Ch2	1uF	I/O (p. 8)	66	c05	Ch2	220nF	Power (p. 2)
12	c73	Cp1	4.7uF	I/O (p. 8)	67	c08	Cpv1	15uF	Power (p. 2)
13	c76	Cv1	4.7nF	I/O (p. 8)	68	c09	Cpv1	15uF	Power (p. 2)
14	c77	Cv1	4.7nF	I/O (p. 8)	69	c10	Cpv1	15uF	Power (p. 2)
15	c78	Cv1	4.7nF	I/O (p. 8)	70	c11	Cpv1	15uF	Power (p. 2)
16	c79	Cv1	4.7nF	I/O (p. 8)	71	c12	Cpv1	15uF	Power (p. 2)
17	c82	Cv1	100nF	I/O (p. 8)	72	c13	Cpv1	15uF	Power (p. 2)
18	c83	Cv1	100nF	I/O (p. 8)	73	c14	Cpv1	15uF	Power (p. 2)
19	c72	Cv2	4.7nF	I/O (p. 8)	74	c15	Cpv1	15uF	Power (p. 2)
20	c75	Cv3	47uF	I/O (p. 8)	75	c16	Cpv1	15uF	Power (p. 2)
21	j3	LCD_Conn		I/O (p. 8)	76	c17	Cpv1	15uF	Power (p. 2)
22	u20	MAX3223CAP		I/O (p. 8)	77	c57	Cpv1	15uF	Power (p. 2)
23	j7	Mic		I/O (p. 8)	78	c58	Cpv1	15uF	Power (p. 2)
24	u19	MiniSIR2		I/O (p. 8)	79	c59	Cpv1	15uF	Power (p. 2)
25	s02	PB2		I/O (p. 8)	80	c60	Cpv1	15uF	Power (p. 2)
26	s03	PB3		I/O (p. 8)	81	c61	Cpv1	15uF	Power (p. 2)
27	s04	PB3		I/O (p. 8)	82	c62	Cpv1	15uF	Power (p. 2)
28	s05	PB4		I/O (p. 8)	83	c03	Cpv2	22uF	Power (p. 2)
29	s06	PB4		I/O (p. 8)	84	c07	Cpv2	100uF	Power (p. 2)
30	s07	PB4		I/O (p. 8)	85	c04	Cv1	100nF	Power (p. 2)
31	s08	PB4		I/O (p. 8)	86	c18	Cv1	100nF	Power (p. 2)
32	s09	PB5		I/O (p. 8)	87	c19	Cv1	100nF	Power (p. 2)
33	s10	PB5		I/O (p. 8)	88	c20	Cv1	100nF	Power (p. 2)
34	s11	PB6		I/O (p. 8)	89	c21	Cv1	100nF	Power (p. 2)
35	p3	Pot2	1M0	I/O (p. 8)	90	c22	Cv1	100nF	Power (p. 2)
36	r23	Rh1	10k0	I/O (p. 8)	91	c23	Cv1	15nF	Power (p. 2)
37	r34	Rh1	1000	I/O (p. 8)	92	c24	Cv1	15nF	Power (p. 2)
38	r35	Rh1	2.2k0	I/O (p. 8)	93	c25	Cv1	10nF	Power (p. 2)
39	r36	Rh1	10k0	I/O (p. 8)	94	c26	Cv1	10nF	Power (p. 2)
40	r37	Rh1	10k0	I/O (p. 8)	95	c27	Cv1	10nF	Power (p. 2)
41	r38	Rh1	10k0	I/O (p. 8)	96	c28	Cv1	10nF	Power (p. 2)
42	r39	Rh1	10k0	I/O (p. 8)	97	c29	Cv1	10nF	Power (p. 2)
43	r40	Rh1	10k0	I/O (p. 8)	98	c30	Cv1	10nF	Power (p. 2)
44	r41	Rh1	10k0	I/O (p. 8)	99	c31	Cv1	10nF	Power (p. 2)
45	r42	Rh1	10k0	I/O (p. 8)	100	c32	Cv1	10nF	Power (p. 2)
46	r43	Rh1	10k0	I/O (p. 8)	101	c33	Cv1	10nF	Power (p. 2)
47	r44	Rh1	10k0	I/O (p. 8)	102	c34	Cv1	10nF	Power (p. 2)
48	r45	Rh1	00	I/O (p. 8)	103	c35	Cv1	10nF	Power (p. 2)
49	r46	Rh1	inf.0	I/O (p. 8)	104	c36	Cv1	10nF	Power (p. 2)
50	r47	Rh1	inf.0	I/O (p. 8)	105	c37	Cv1	10nF	Power (p. 2)
51	j5	RS_Conn		I/O (p. 8)	106	c38	Cv1	10nF	Power (p. 2)
52	r48	Rv2	1.30	I/O (p. 8)	107	c39	Cv1	10nF	Power (p. 2)
53	j8	Spkr		I/O (p. 8)	108	c40	Cv1	10nF	Power (p. 2)
54	j4	TS_Conn		I/O (p. 8)	109	c41	Cv1	10nF	Power (p. 2)

Table 8: Itsy mother-board version 1.5: component list (sorted by component numbers).

¹⁸The layout and component lists of the Itsy mother-board version 1.1 are not included.

The Itsy Pocket Computer Version 1.5: Hardware Description

No.	Ref.	Component Schematic body	Value	Schematic	No.	Ref.	Component Schematic body	Value	Schematic
110	c42	Cv1	10nF	Power (p. 2)	170	t04	TP		Power (p. 2)
111	c43	Cv1	10nF	Power (p. 2)	171	t05	TP		Power (p. 2)
112	c44	Cv1	10nF	Power (p. 2)	172	t06	TP		Power (p. 2)
113	c45	Cv1	6.8nF	Power (p. 2)	173	t07	TP		Power (p. 2)
114	c46	Cv1	10nF	Power (p. 2)	174	t08	TP		Power (p. 2)
115	c47	Cv1	10nF	Power (p. 2)	175	t09	TP		Power (p. 2)
116	c48	Cv1	6.8nF	Power (p. 2)	176	t10	TP		Power (p. 2)
117	c49	Cv1	10nF	Power (p. 2)	177	t11	TP		Power (p. 2)
118	c50	Cv1	10nF	Power (p. 2)	178	v01	Via		Power (p. 2)
119	c51	Cv1	10nF	Power (p. 2)	179	v02	Via		Power (p. 2)
120	c52	Cv1	10nF	Power (p. 2)	180	v03	Via		Power (p. 2)
121	c53	Cv1	10nF	Power (p. 2)	181	v04	Via		Power (p. 2)
122	c54	Cv1	10nF	Power (p. 2)	182	v05	Via		Power (p. 2)
123	c55	Cv1	10nF	Power (p. 2)	183	v06	Via		Power (p. 2)
124	c56	Cv1	10nF	Power (p. 2)	184	v07	Via		Power (p. 2)
125	c63	Cv1	100nF	Power (p. 2)	185	v08	Via		Power (p. 2)
126	c64	Cv1	10nF	Power (p. 2)	186	v09	Via		Power (p. 2)
127	c65	Cv1	10nF	Power (p. 2)	187	v10	Via		Power (p. 2)
128	c66	Cv1	10nF	Power (p. 2)	188	v11	Via		Power (p. 2)
129	c67	Cv1	10nF	Power (p. 2)	189	v12	Via		Power (p. 2)
130	c68	Cv1	10nF	Power (p. 2)	190	v13	Via		Power (p. 2)
131	c69	Cv1	10nF	Power (p. 2)	191	v14	Via		Power (p. 2)
132	c70	Cv1	10nF	Power (p. 2)	192	v15	Via		Power (p. 2)
133	c71	Cv1	10nF	Power (p. 2)	193	v16	Via		Power (p. 2)
134	l1	Lh	10uH	Power (p. 2)	194	v17	Via		Power (p. 2)
135	u03	MAX793RCSE		Power (p. 2)	195	v18	Via		Power (p. 2)
136	u01	MAX849ESE		Power (p. 2)	196	v19	Via		Power (p. 2)
137	u02	MIC29152BU		Power (p. 2)	197	v20	Via		Power (p. 2)
138	s01	PB1		Power (p. 2)	198	v21	Via		Power (p. 2)
139	s12	PB5		Power (p. 2)	199	v22	Via		Power (p. 2)
140	p1	Pot1	20k0	Power (p. 2)	200	v23	Via		Power (p. 2)
141	p2	Pot1	500k0	Power (p. 2)	201	v24	Via		Power (p. 2)
142	r04	Rh1	100	Power (p. 2)	202	v25	Via		Power (p. 2)
143	r10	Rh1	inf.0	Power (p. 2)	203	v26	Via		Power (p. 2)
144	r11	Rh1	00	Power (p. 2)	204	v27	Via		Power (p. 2)
145	r14	Rh1	inf.0	Power (p. 2)	205	v28	Via		Power (p. 2)
146	r15	Rh1	00	Power (p. 2)	206	u08b	PZ3032.8A44		PZ3032 (p. 4)
147	r03	Rh2	20m0	Power (p. 2)	207	u08a	PZ3032.8BC		PZ3032 (p. 4)
148	r49	Rh2	20m0	Power (p. 2)	208	r24	Rh1	30k0	Proc (p. 3)
149	r50	Rh2	20m0	Power (p. 2)	209	r25	Rh1	36k0	Proc (p. 3)
150	r01	Rv1	2M0	Power (p. 2)	210	r26	Rh1	30k0	Proc (p. 3)
151	r02	Rv1	2M0	Power (p. 2)	211	r27	Rh1	12k0	Proc (p. 3)
152	r05	Rv1	100k0	Power (p. 2)	212	r28	Rh1	12k0	Proc (p. 3)
153	r06	Rv1	100k0	Power (p. 2)	213	r29	Rh1	20k0	Proc (p. 3)
154	r07	Rv1	56k0	Power (p. 2)	214	r30	Rh1	36k0	Proc (p. 3)
155	r08	Rv1	133k0	Power (p. 2)	215	r31	Rh1	36k0	Proc (p. 3)
156	r09	Rv1	100k0	Power (p. 2)	216	r19	Rv1	10k0	Proc (p. 3)
157	r12	Rv1	100k0	Power (p. 2)	217	r20	Rv1	10k0	Proc (p. 3)
158	r13	Rv1	147k0	Power (p. 2)	218	r21	Rv1	56k0	Proc (p. 3)
159	r16	Rv1	56k0	Power (p. 2)	219	r22	Rv1	56k0	Proc (p. 3)
160	r17	Rv1	100k0	Power (p. 2)	220	r51	Rv1	00	Proc (p. 3)
161	r18	Rv1	4.7k0	Power (p. 2)	221	u06	SA_1100		Proc (p. 3)
162	c01	SC	0.33F	Power (p. 2)	222	u07	SG_8002JC.MCC	1MHz	Proc (p. 3)
163	c02	SC	0.33F	Power (p. 2)	223	t12	TP		Proc (p. 3)
164	d1	SD	MBR0520L	Power (p. 2)	224	t13	TP		Proc (p. 3)
165	u04	TC7SL04FU		Power (p. 2)	225	t14	TP		Proc (p. 3)
166	u05	TC7SL04FU		Power (p. 2)	226	t15	TP		Proc (p. 3)
167	t01	TP		Power (p. 2)	227	x1	Xtal1	3.6864MHz	Proc (p. 3)
168	t02	TP		Power (p. 2)	228	x2	Xtal2	32.768kHz	Proc (p. 3)
169	t03	TP		Power (p. 2)					

Table 8: Itsy mother-board version 1.5: component list (sorted by component numbers).

The Itsy Pocket Computer Version 1.5: Hardware Description

Component					Component				
Ref.	Schematic body	Value	No.	Schematic	Ref.	Schematic body	Value	No.	Schematic
c01	SC	0.33F	162	Power (p. 2)	c68	Cv1	10nF	130	Power (p. 2)
c02	SC	0.33F	163	Power (p. 2)	c69	Cv1	10nF	131	Power (p. 2)
c03	Cpv2	22uF	83	Power (p. 2)	c70	Cv1	10nF	132	Power (p. 2)
c04	Cv1	100nF	85	Power (p. 2)	c71	Cv1	10nF	133	Power (p. 2)
c05	Ch2	220nF	66	Power (p. 2)	c72	Cv2	4.7nF	19	IO (p. 8)
c06	Ch1	100nF	65	Power (p. 2)	c73	Cph1	4.7uF	12	IO (p. 8)
c07	Cpv2	100uF	84	Power (p. 2)	c74	Ch2	1uF	11	IO (p. 8)
c08	Cpv1	15uF	67	Power (p. 2)	c75	Cv3	47uF	20	IO (p. 8)
c09	Cpv1	15uF	68	Power (p. 2)	c76	Cv1	4.7nF	13	IO (p. 8)
c10	Cpv1	15uF	69	Power (p. 2)	c77	Cv1	4.7nF	14	IO (p. 8)
c11	Cpv1	15uF	70	Power (p. 2)	c78	Cv1	4.7nF	15	IO (p. 8)
c12	Cpv1	15uF	71	Power (p. 2)	c79	Cv1	4.7nF	16	IO (p. 8)
c13	Cpv1	15uF	72	Power (p. 2)	c80	Ch1	100nF	9	IO (p. 8)
c14	Cpv1	15uF	73	Power (p. 2)	c81	Ch1	100nF	10	IO (p. 8)
c15	Cpv1	15uF	74	Power (p. 2)	c82	Cv1	100nF	17	IO (p. 8)
c16	Cpv1	15uF	75	Power (p. 2)	c83	Cv1	100nF	18	IO (p. 8)
c17	Cpv1	15uF	76	Power (p. 2)	d1	SD	MBR0520L	164	Power (p. 2)
c18	Cv1	100nF	86	Power (p. 2)	j1	Batt		64	Power (p. 2)
c19	Cv1	100nF	87	Power (p. 2)	j2	DC.Conn		2	DCIntf (p. 6)
c20	Cv1	100nF	88	Power (p. 2)	j3	LCD.Conn		21	IO (p. 8)
c21	Cv1	100nF	89	Power (p. 2)	j4	TS.Conn		54	IO (p. 8)
c22	Cv1	100nF	90	Power (p. 2)	j5	RS.Conn		51	IO (p. 8)
c23	Cv1	15nF	91	Power (p. 2)	j6	Audio.Conn		8	IO (p. 8)
c24	Cv1	15nF	92	Power (p. 2)	j7	Mic		23	IO (p. 8)
c25	Cv1	10nF	93	Power (p. 2)	j8	Spkr		53	IO (p. 8)
c26	Cv1	10nF	94	Power (p. 2)	l1	Lh	10uH	134	Power (p. 2)
c27	Cv1	10nF	95	Power (p. 2)	p1	Pot1	20k0	140	Power (p. 2)
c28	Cv1	10nF	96	Power (p. 2)	p2	Pot1	500k0	141	Power (p. 2)
c29	Cv1	10nF	97	Power (p. 2)	p3	Pot2	1M0	35	IO (p. 8)
c30	Cv1	10nF	98	Power (p. 2)	r01	Rv1	2M0	150	Power (p. 2)
c31	Cv1	10nF	99	Power (p. 2)	r02	Rv1	2M0	151	Power (p. 2)
c32	Cv1	10nF	100	Power (p. 2)	r03	Rh2	20m0	147	Power (p. 2)
c33	Cv1	10nF	101	Power (p. 2)	r04	Rh1	100	142	Power (p. 2)
c34	Cv1	10nF	102	Power (p. 2)	r05	Rv1	100k0	152	Power (p. 2)
c35	Cv1	10nF	103	Power (p. 2)	r06	Rv1	100k0	153	Power (p. 2)
c36	Cv1	10nF	104	Power (p. 2)	r07	Rv1	56k0	154	Power (p. 2)
c37	Cv1	10nF	105	Power (p. 2)	r08	Rv1	133k0	155	Power (p. 2)
c38	Cv1	10nF	106	Power (p. 2)	r09	Rv1	100k0	156	Power (p. 2)
c39	Cv1	10nF	107	Power (p. 2)	r10	Rh1	inf.0	143	Power (p. 2)
c40	Cv1	10nF	108	Power (p. 2)	r11	Rh1	00	144	Power (p. 2)
c41	Cv1	10nF	109	Power (p. 2)	r12	Rv1	100k0	157	Power (p. 2)
c42	Cv1	10nF	110	Power (p. 2)	r13	Rv1	147k0	158	Power (p. 2)
c43	Cv1	10nF	111	Power (p. 2)	r14	Rh1	inf.0	145	Power (p. 2)
c44	Cv1	10nF	112	Power (p. 2)	r15	Rh1	00	146	Power (p. 2)
c45	Cv1	6.8nF	113	Power (p. 2)	r16	Rv1	56k0	159	Power (p. 2)
c46	Cv1	10nF	114	Power (p. 2)	r17	Rv1	100k0	160	Power (p. 2)
c47	Cv1	10nF	115	Power (p. 2)	r18	Rv1	4.7k0	161	Power (p. 2)
c48	Cv1	6.8nF	116	Power (p. 2)	r19	Rv1	10k0	216	Proc (p. 3)
c49	Cv1	10nF	117	Power (p. 2)	r20	Rv1	10k0	217	Proc (p. 3)
c50	Cv1	10nF	118	Power (p. 2)	r21	Rv1	56k0	218	Proc (p. 3)
c51	Cv1	10nF	119	Power (p. 2)	r22	Rv1	56k0	219	Proc (p. 3)
c52	Cv1	10nF	120	Power (p. 2)	r23	Rh1	10k0	36	IO (p. 8)
c53	Cv1	10nF	121	Power (p. 2)	r24	Rh1	30k0	208	Proc (p. 3)
c54	Cv1	10nF	122	Power (p. 2)	r25	Rh1	36k0	209	Proc (p. 3)
c55	Cv1	10nF	123	Power (p. 2)	r26	Rh1	30k0	210	Proc (p. 3)
c56	Cv1	10nF	124	Power (p. 2)	r27	Rh1	12k0	211	Proc (p. 3)
c57	Cpv1	15uF	77	Power (p. 2)	r28	Rh1	12k0	212	Proc (p. 3)
c58	Cpv1	15uF	78	Power (p. 2)	r29	Rh1	20k0	213	Proc (p. 3)
c59	Cpv1	15uF	79	Power (p. 2)	r30	Rh1	36k0	214	Proc (p. 3)
c60	Cpv1	15uF	80	Power (p. 2)	r31	Rh1	36k0	215	Proc (p. 3)
c61	Cpv1	15uF	81	Power (p. 2)	r32	Rv1	inf.0	3	DCIntf (p. 6)
c62	Cpv1	15uF	82	Power (p. 2)	r33	Rv1	inf.0	4	DCIntf (p. 6)
c63	Cv1	100nF	125	Power (p. 2)	r34	Rh1	1000	37	IO (p. 8)
c64	Cv1	10nF	126	Power (p. 2)	r35	Rh1	2.2k0	38	IO (p. 8)
c65	Cv1	10nF	127	Power (p. 2)	r36	Rh1	10k0	39	IO (p. 8)
c66	Cv1	10nF	128	Power (p. 2)	r37	Rh1	10k0	40	IO (p. 8)
c67	Cv1	10nF	129	Power (p. 2)	r38	Rh1	10k0	41	IO (p. 8)

Table 9: Itsy mother-board version 1.5: component list (sorted by component references).

The Itsy Pocket Computer Version 1.5: Hardware Description

Component					Component				
Ref.	Schematic body	Value	No.	Schematic	Ref.	Schematic body	Value	No.	Schematic
r39	Rh1	10k0	42	IO (p. 8)	u05	TC7SL04FU		166	Power (p. 2)
r40	Rh1	10k0	43	IO (p. 8)	u06	SA_1100		221	Proc (p. 3)
r41	Rh1	10k0	44	IO (p. 8)	u07	SG_8002JC_MCC	1MHz	222	Proc (p. 3)
r42	Rh1	10k0	45	IO (p. 8)	u08a	PZ3032_8BC		207	PZ3032 (p. 4)
r43	Rh1	10k0	46	IO (p. 8)	u08b	PZ3032_8A44		206	PZ3032 (p. 4)
r44	Rh1	10k0	47	IO (p. 8)	u09	XX29xxxT		59	Memory (p. 5)
r45	Rh1	00	48	IO (p. 8)	u10	XX29xxxR		58	Memory (p. 5)
r46	Rh1	inf.0	49	IO (p. 8)	u11	XX516516x		60	Memory (p. 5)
r47	Rh1	inf.0	50	IO (p. 8)	u12	XX516516x		61	Memory (p. 5)
r48	Rv2	1.30	52	IO (p. 8)	u13	SN74LVCH16244ADGG		5	DCIntf (p. 6)
r49	Rh2	20m0	148	Power (p. 2)	u14	SN74LVCH16244ADGG		6	DCIntf (p. 6)
r50	Rh2	20m0	149	Power (p. 2)	u15	SN74LVCH16244ADGG		7	DCIntf (p. 6)
r51	Rv1	00	220	Proc (p. 3)	u16	SN74LVCH16245ADGG		0	DataBuf (p. 7)
r52	Rh1	10k0	56	Memory (p. 5)	u17	SN74LVCH16245ADGG		1	DataBuf (p. 7)
r53	Rh1	10k0	57	Memory (p. 5)	u18	UCB1200		55	IO (p. 8)
s1	Mnt		62	Itsy (p. 1)	u19	MiniSIR2		24	IO (p. 8)
s2	Mnt		63	Itsy (p. 1)	u20	MAX3223CAP		22	IO (p. 8)
s01	PB1		138	Power (p. 2)	v01	Via		178	Power (p. 2)
s02	PB2		25	IO (p. 8)	v02	Via		179	Power (p. 2)
s03	PB3		26	IO (p. 8)	v03	Via		180	Power (p. 2)
s04	PB3		27	IO (p. 8)	v04	Via		181	Power (p. 2)
s05	PB4		28	IO (p. 8)	v05	Via		182	Power (p. 2)
s06	PB4		29	IO (p. 8)	v06	Via		183	Power (p. 2)
s07	PB4		30	IO (p. 8)	v07	Via		184	Power (p. 2)
s08	PB4		31	IO (p. 8)	v08	Via		185	Power (p. 2)
s09	PB5		32	IO (p. 8)	v09	Via		186	Power (p. 2)
s10	PB5		33	IO (p. 8)	v10	Via		187	Power (p. 2)
s11	PB6		34	IO (p. 8)	v11	Via		188	Power (p. 2)
s12	PB5		139	Power (p. 2)	v12	Via		189	Power (p. 2)
t01	TP		167	Power (p. 2)	v13	Via		190	Power (p. 2)
t02	TP		168	Power (p. 2)	v14	Via		191	Power (p. 2)
t03	TP		169	Power (p. 2)	v15	Via		192	Power (p. 2)
t04	TP		170	Power (p. 2)	v16	Via		193	Power (p. 2)
t05	TP		171	Power (p. 2)	v17	Via		194	Power (p. 2)
t06	TP		172	Power (p. 2)	v18	Via		195	Power (p. 2)
t07	TP		173	Power (p. 2)	v19	Via		196	Power (p. 2)
t08	TP		174	Power (p. 2)	v20	Via		197	Power (p. 2)
t09	TP		175	Power (p. 2)	v21	Via		198	Power (p. 2)
t10	TP		176	Power (p. 2)	v22	Via		199	Power (p. 2)
t11	TP		177	Power (p. 2)	v23	Via		200	Power (p. 2)
t12	TP		223	Proc (p. 3)	v24	Via		201	Power (p. 2)
t13	TP		224	Proc (p. 3)	v25	Via		202	Power (p. 2)
t14	TP		225	Proc (p. 3)	v26	Via		203	Power (p. 2)
t15	TP		226	Proc (p. 3)	v27	Via		204	Power (p. 2)
u01	MAX849ESE		136	Power (p. 2)	v28	Via		205	Power (p. 2)
u02	MIC29152BU		137	Power (p. 2)	x1	Xtal1	3.6864MHz	227	Proc (p. 3)
u03	MAX793RCSE		135	Power (p. 2)	x2	Xtal2	32.768kHz	228	Proc (p. 3)
u04	TC7SL04FU		165	Power (p. 2)					

Table 9: Itsy mother-board version 1.5: component list (sorted by component references).

The Itsy Pocket Computer Version 1.5: Hardware Description

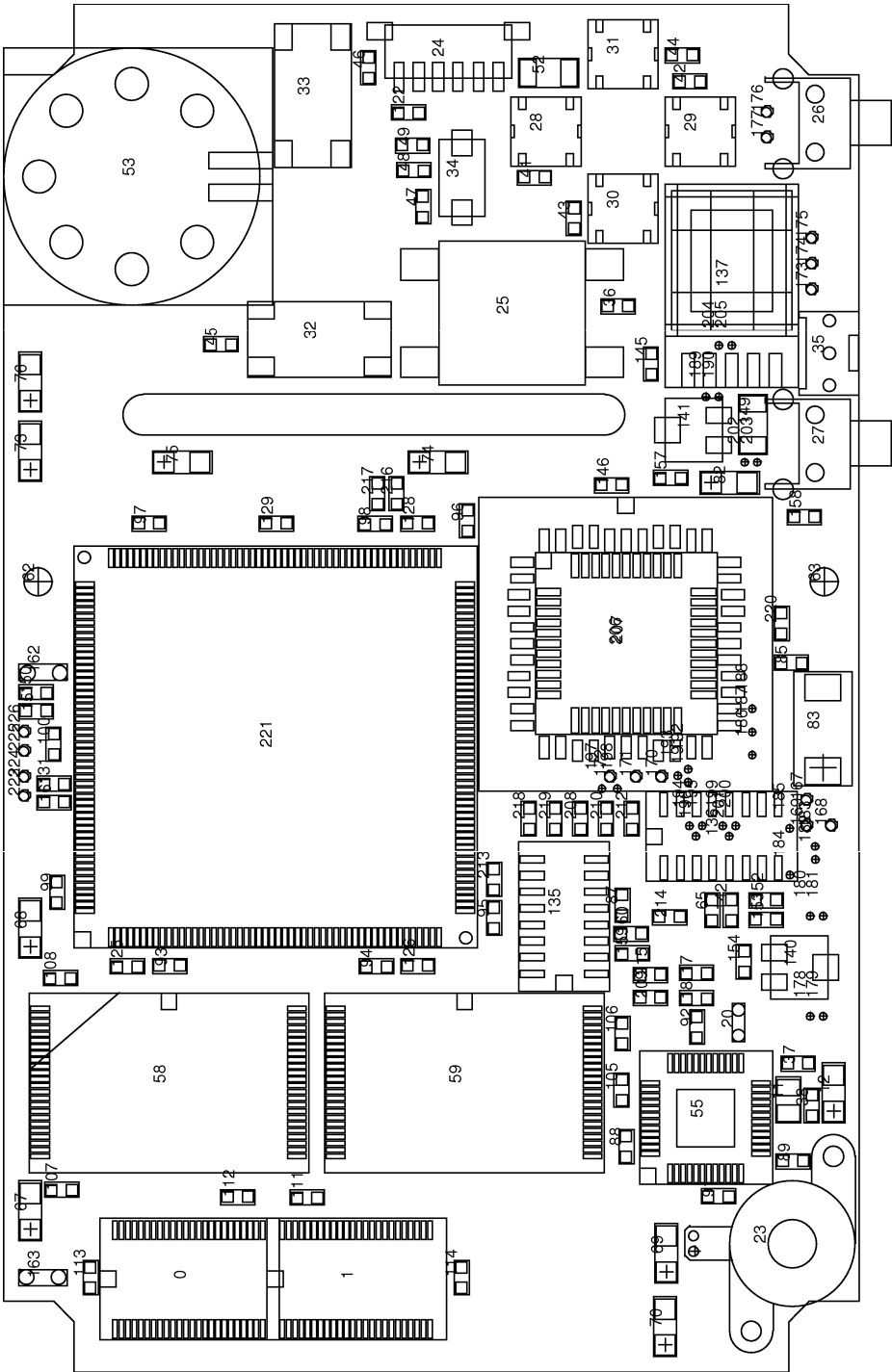


Figure 10: Itsy mother-board version 1.5: top-side PCB layout.

The Itsy Pocket Computer Version 1.5: Hardware Description

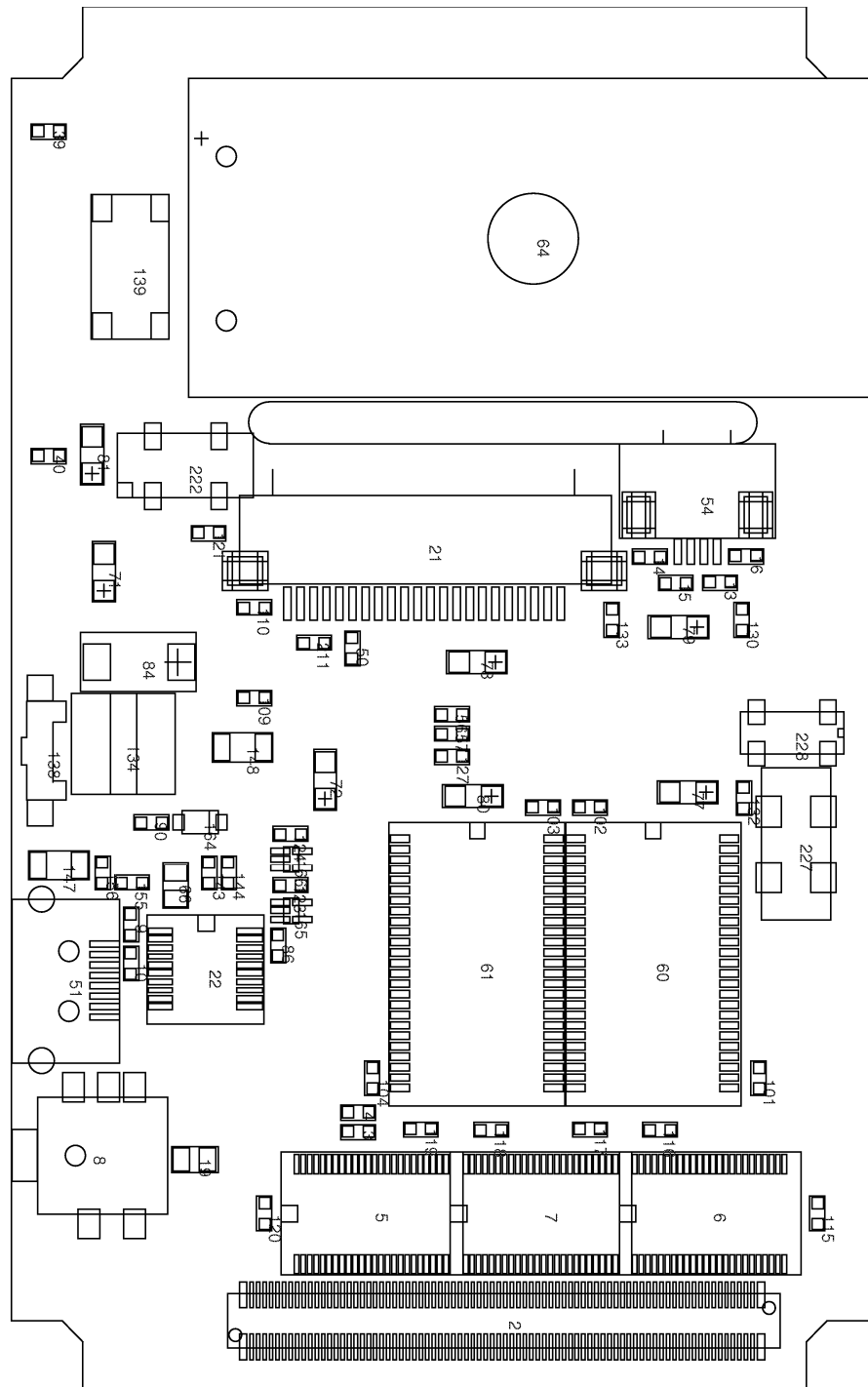


Figure 11: Itsy mother-board version 1.5: bottom-side PCB layout.